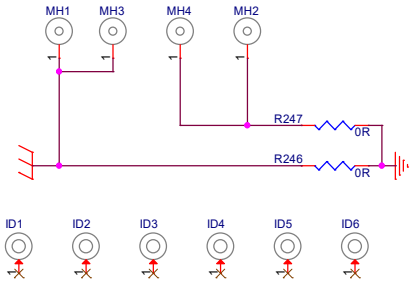
ET6ULL BB

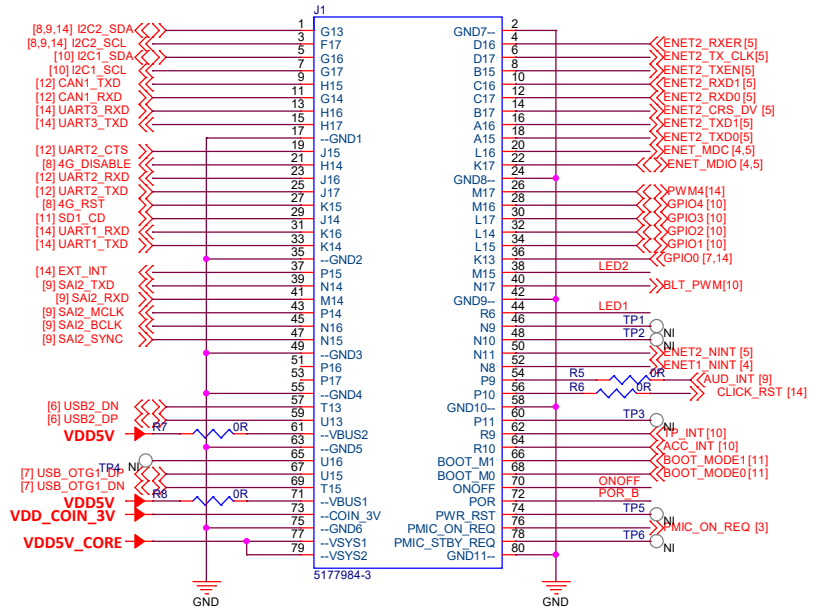
Table of Content

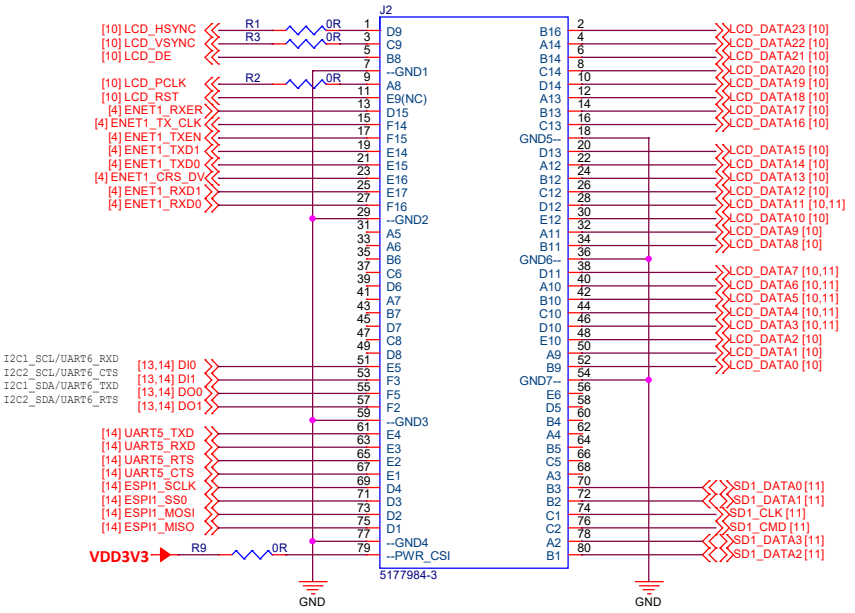
Revision History

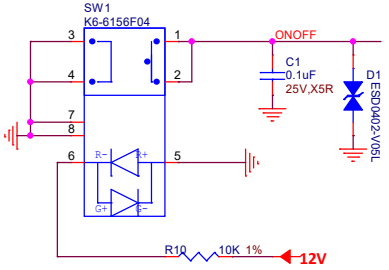
Rev. Code	Date	By	Description
Rev:00	2018-11-30	Jake	First version

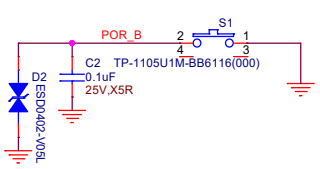


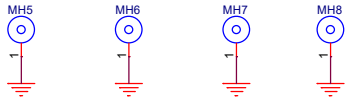
	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Friday, March 25, 2022	Sheet: 1 of 14

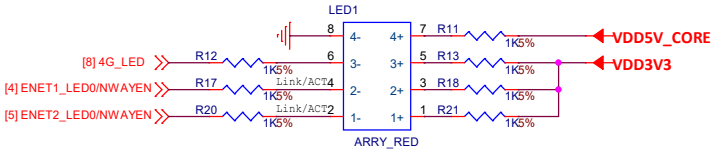


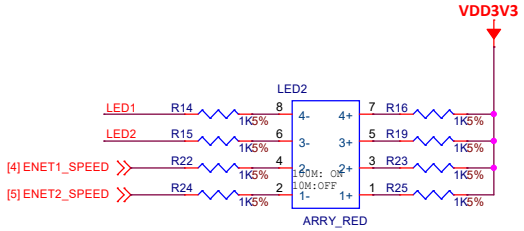




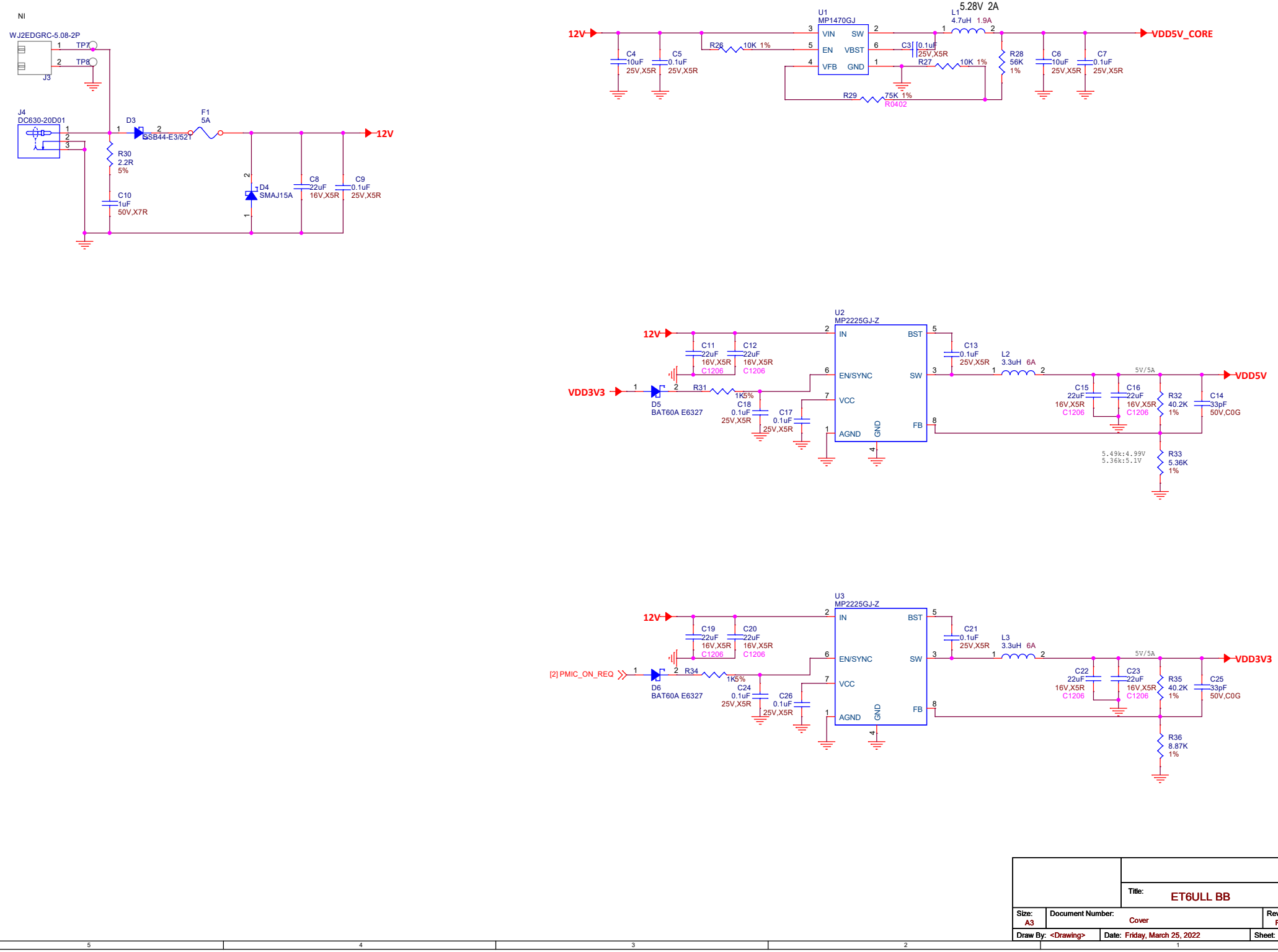




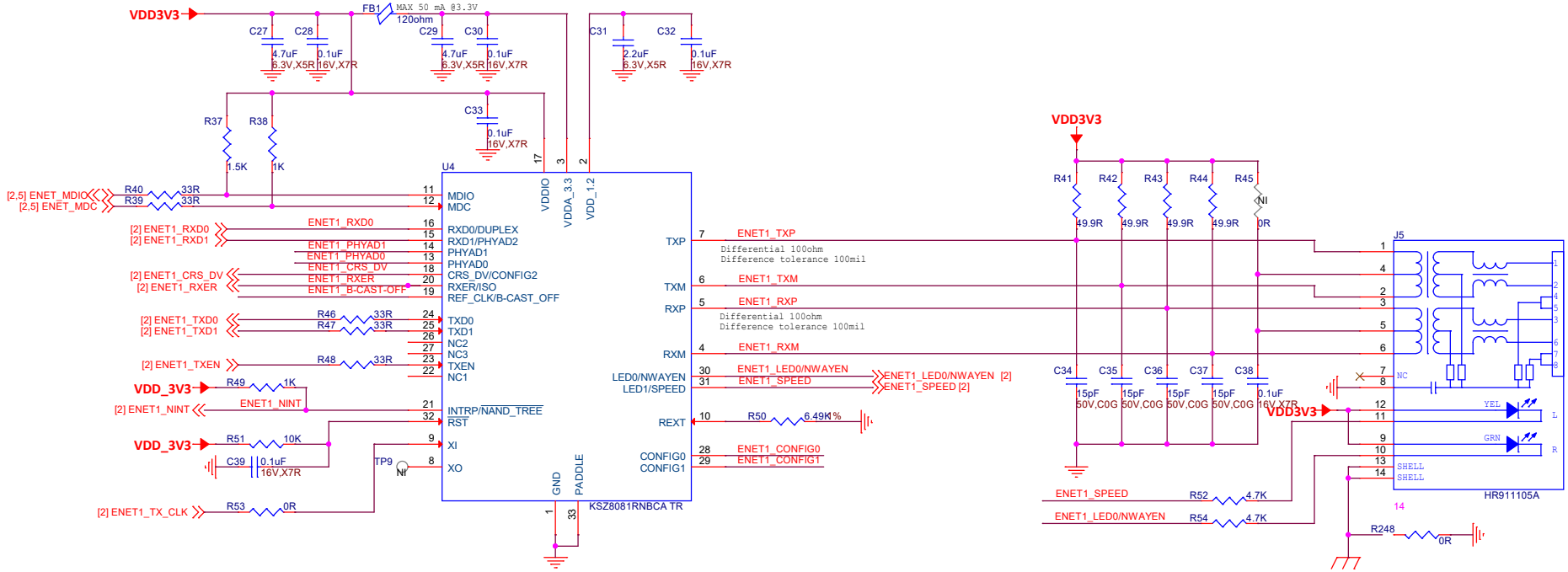


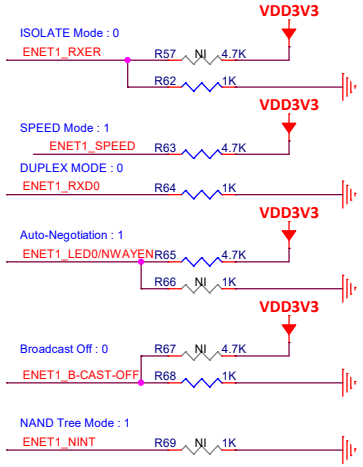


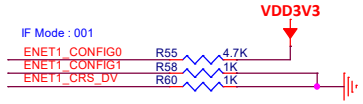
	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Friday, March 25, 2022	Sheet: 2 of 14

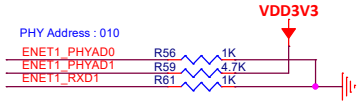

NI
WJ2EDGRC-5.08-2P
J3
TP7
TP8
J4
DC630-20D01
D3
SSB44-E3/52T
F1
5A
12V
R30
2.2R
5%
C10
1uF
50V,X7R
D4
SMAJ15A
C8
22uF
16V,X5R
C9
0.1uF
25V,X5R
U1
MP1470GJ
VIN
SW
EN
VBST
VFB
GND
C4
10uF
25V,X5R
C5
0.1uF
25V,X5R
R26
10K 1%
C3
0.1uF
25V,X5R
R27
10K 1%
R29
75K 1%
R0402
L1
4.7uH 1.9A
5.28V 2A
R28
56K
1%
C6
10uF
25V,X5R
C7
0.1uF
25V,X5R
VDD5V_CORE
U2
MP2225GJ-Z
IN
BST
EN/SYNC
SW
VCC
AGND
GND
FB
C11
22uF
16V,X5R
C1206
C12
22uF
16V,X5R
C1206
VDD3V3
D5
BAT60A E6327
R31
1K5%
C18
0.1uF
25V,X5R
C17
0.1uF
25V,X5R
C13
0.1uF
25V,X5R
L2
3.3uH 6A
5V/5A
C15
22uF
16V,X5R
C1206
C16
22uF
16V,X5R
C1206
R32
40.2K
1%
C14
33pF
50V,C0G
5.49k:4.99V
5.36k:5.1V
R33
5.36K
1%
VDD5V
U3
MP2225GJ-Z
C19
22uF
16V,X5R
C1206
C20
22uF
16V,X5R
C1206
[2] PMIC_ON_REQ
D6
BAT60A E6327
R34
1K5%
C24
0.1uF
25V,X5R
C26
0.1uF
25V,X5R
C21
0.1uF
25V,X5R
L3
3.3uH 6A
5V/5A
C22
22uF
16V,X5R
C1206
C23
22uF
16V,X5R
C1206
R35
40.2K
1%
C25
33pF
50V,C0G
R36
8.87K
1%
VDD3V3
Title: ET6ULL BB
Size: A3
Document Number: Cover
Rev: Rev0.0
Draw By: <Drawing>
Date: Friday, March 25, 2022
Sheet: 3 of 14

10/100Mbps Ethernet Circuit





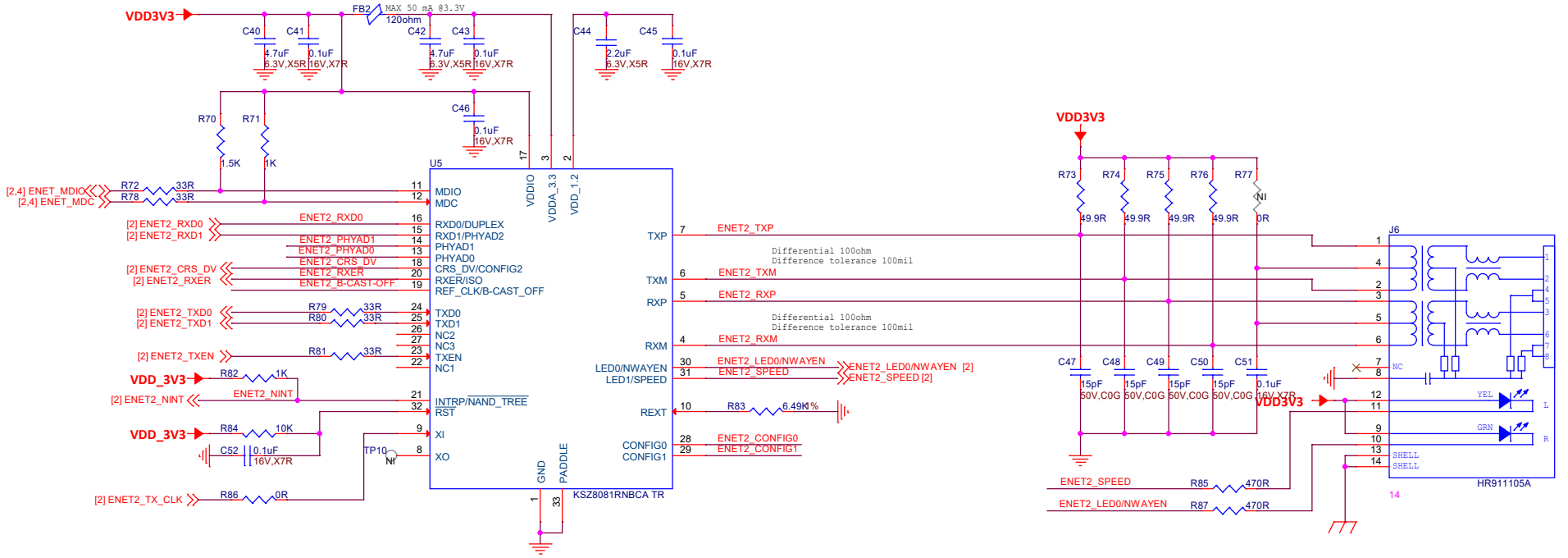


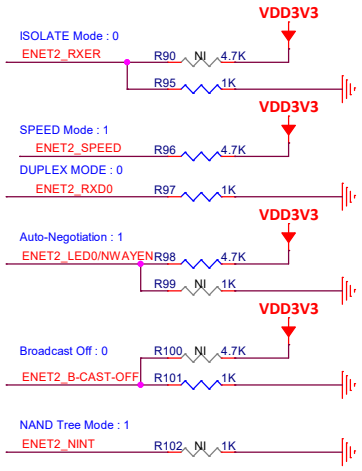


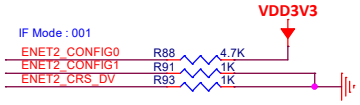
# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

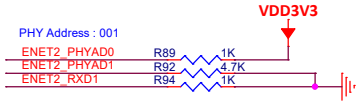
# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

Title: ET6ULL BB		
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Friday, March 25, 2022	Sheet: 4 of 14







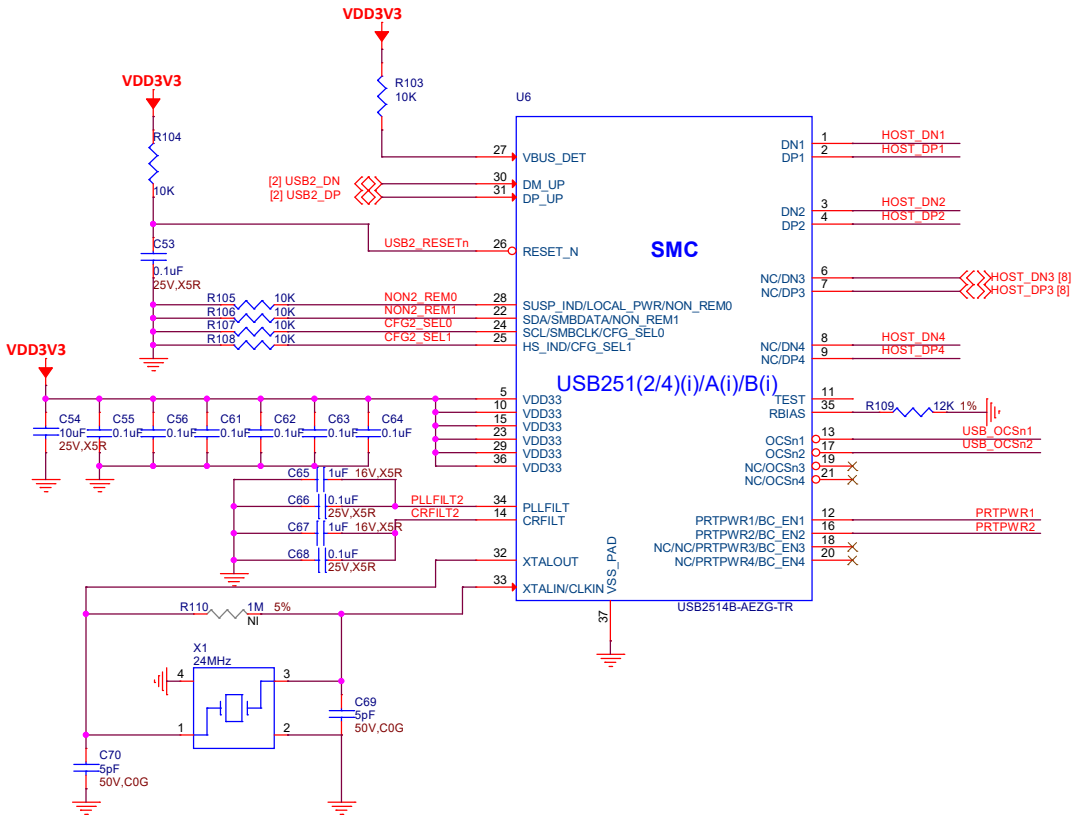


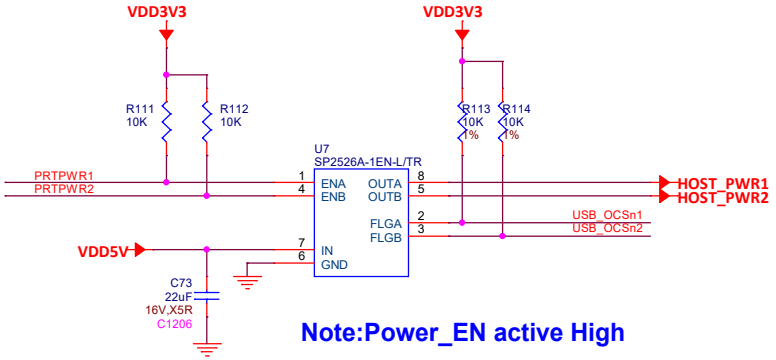
# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

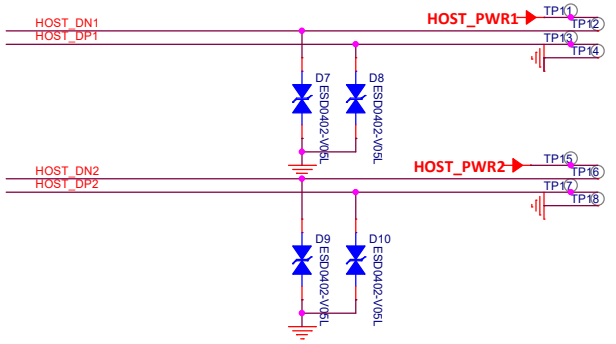
	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Friday, March 25, 2022	Sheet: 5 of 14

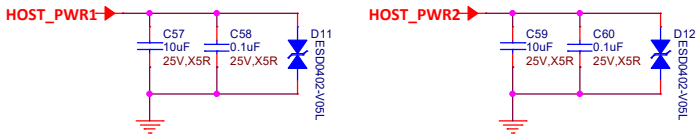
USB HOST

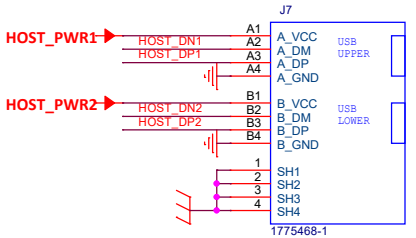


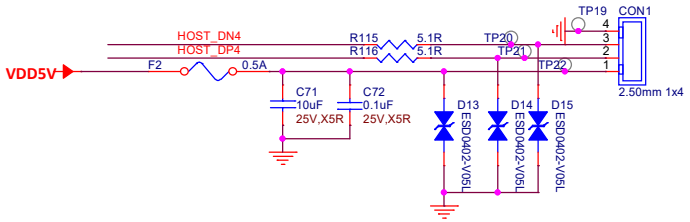


Note:Power_EN active High



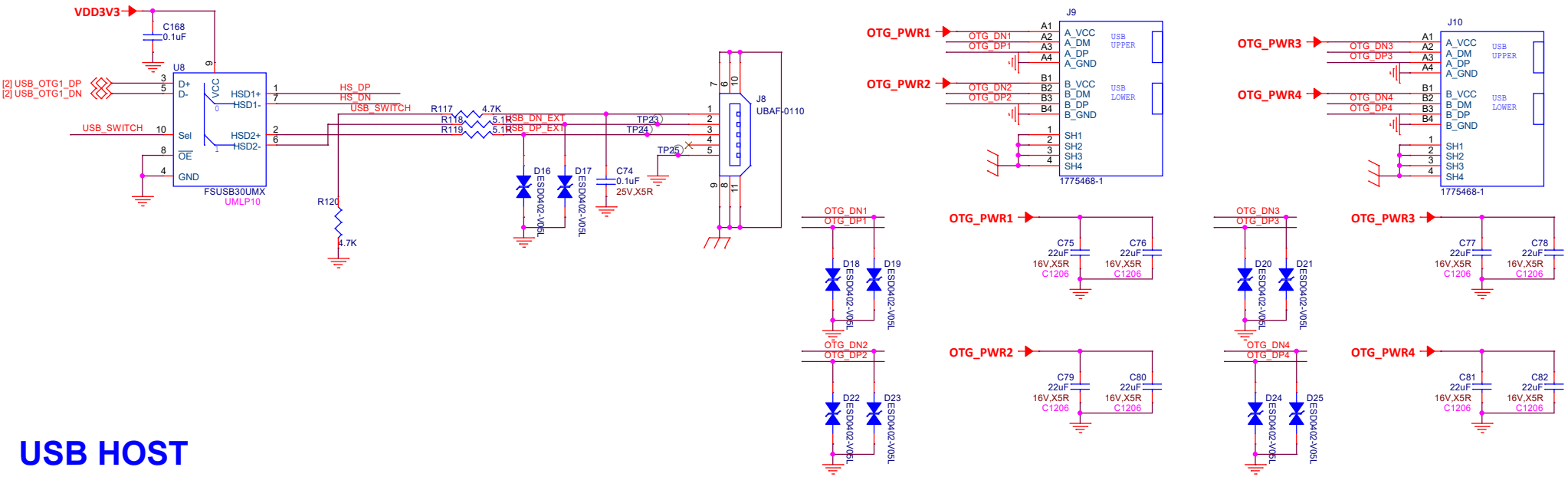


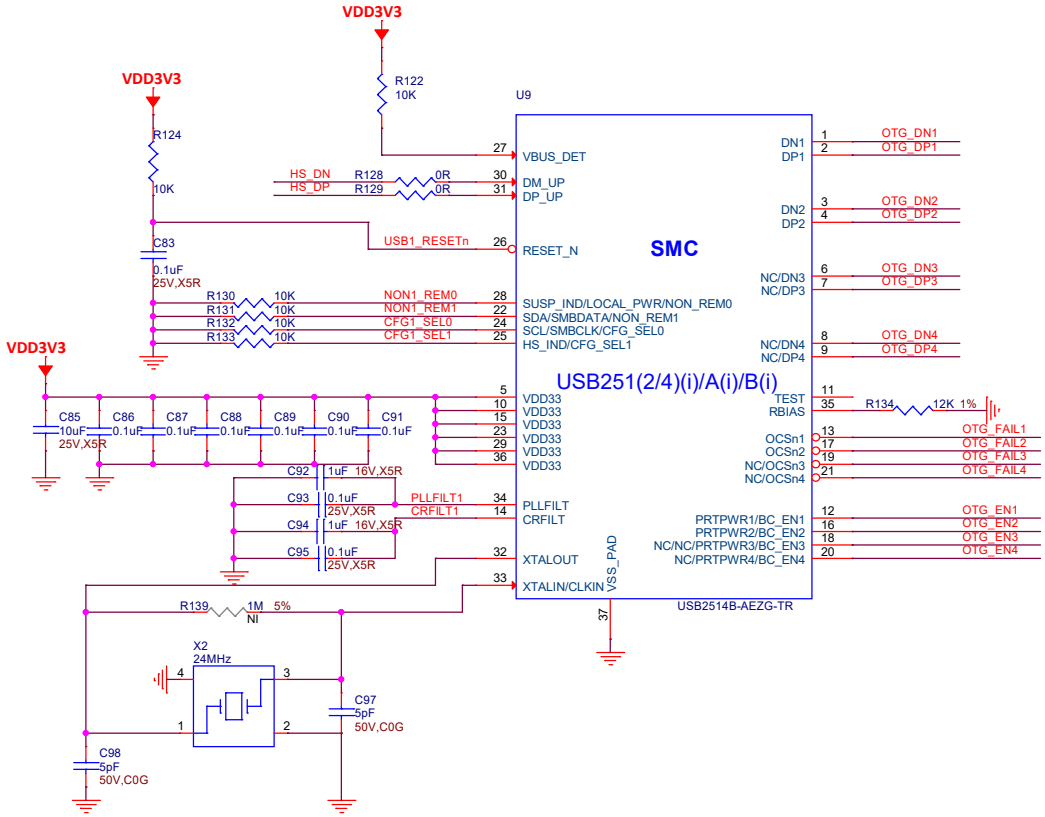


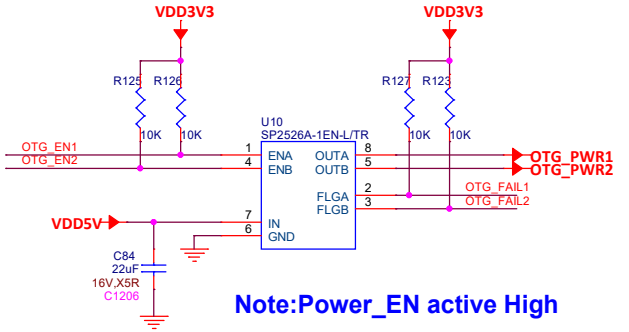


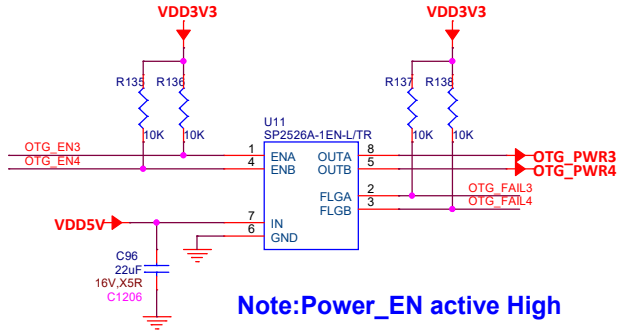
	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Friday, March 25, 2022	Sheet: 6 of 14

USB HOST



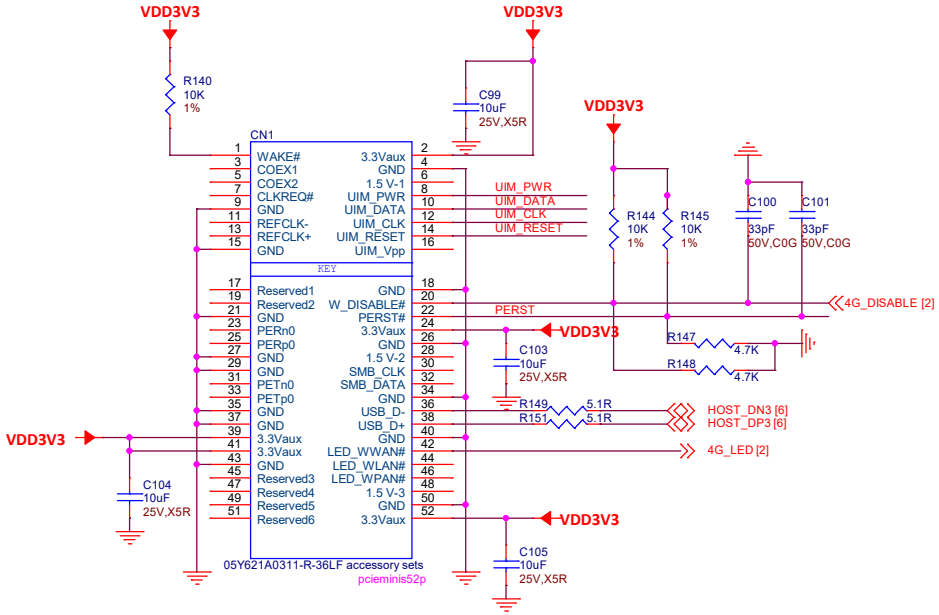


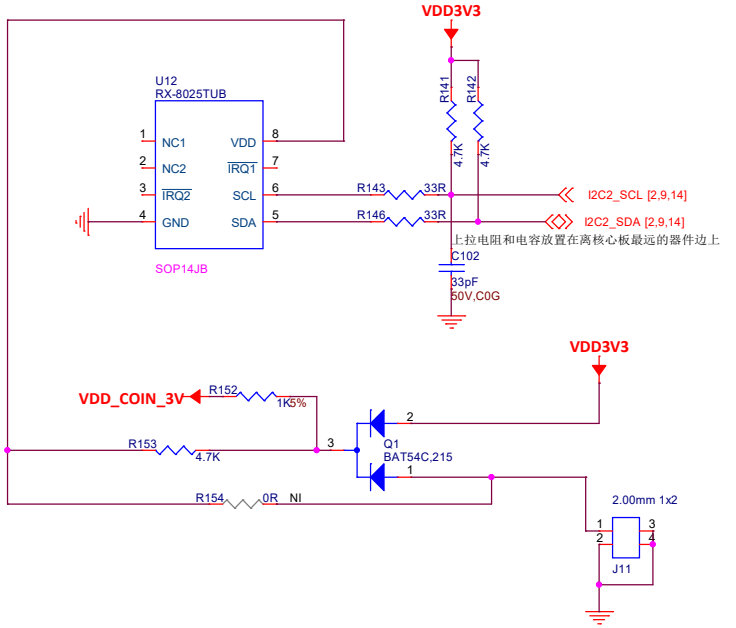


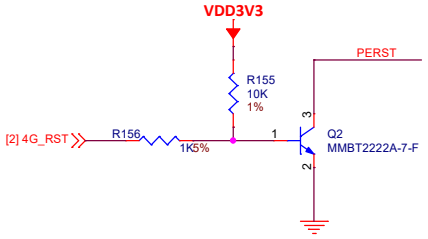


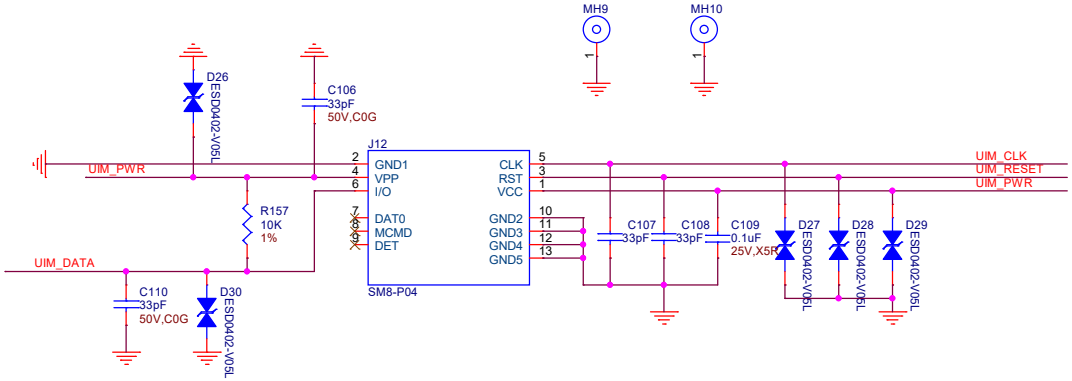
	Title: <Title>	
Size: A3	Document Number: <Doc>	Rev: Rev0.0
Draw By: <Drawing>	Date: Monday, July 04, 2022	Sheet: 7 of 14

PCIE



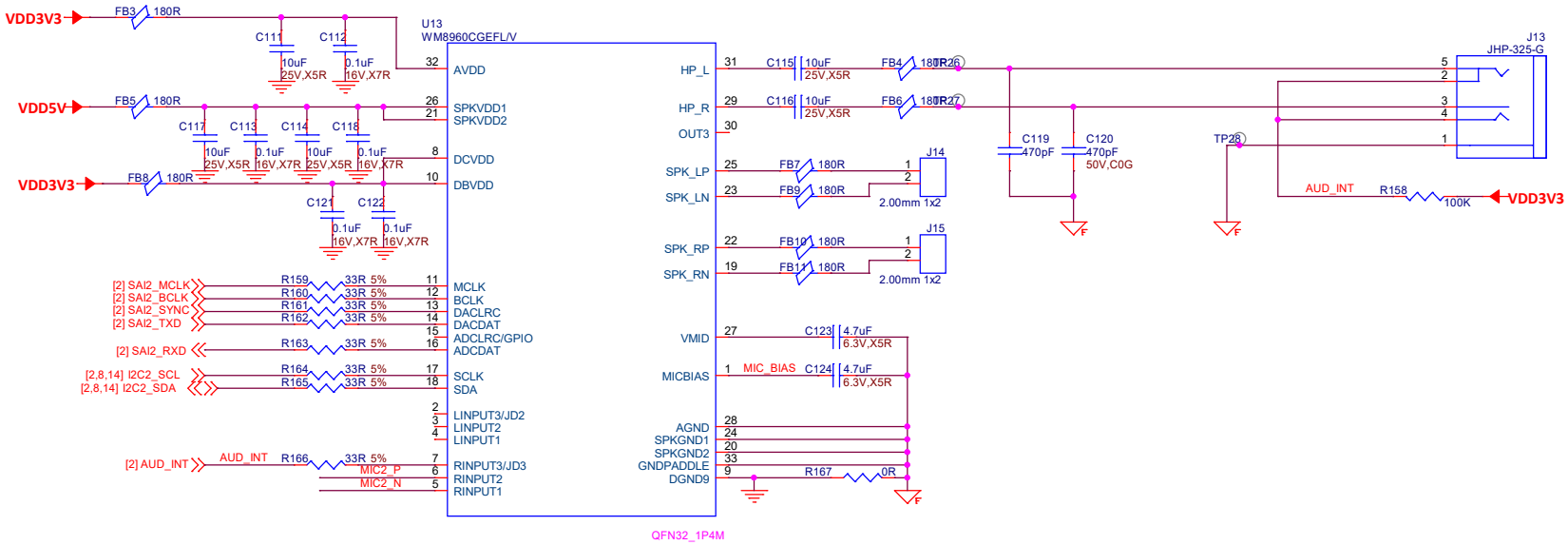




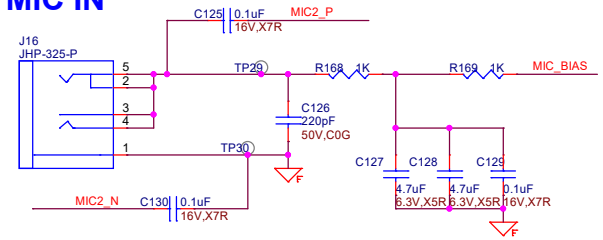


Title:	ET6ULL BB
Size: A3	Document Number: Cover
Rev: Rev0.0	
Draw By: <Drawing>	Date: Friday, March 25, 2022
Sheet: 8 of 14	

AUDIO



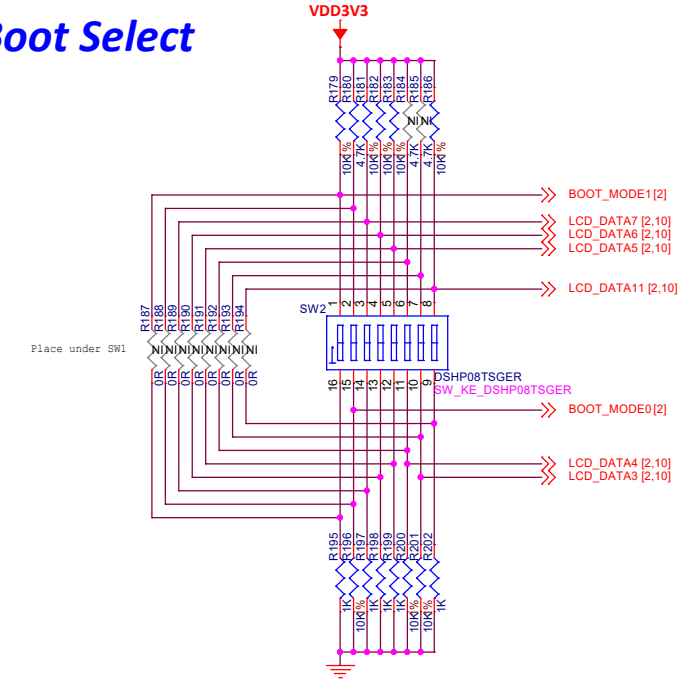
MIC IN



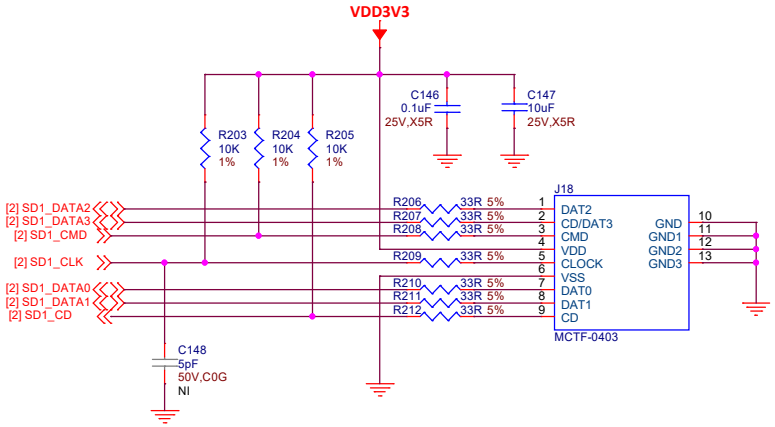
	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Monday, July 04, 2022	Sheet: 9 of 14


U14
SN74AVCA164245GR
U15
SN74AVCA164245GR
RESAR_IS_4/SM
J17
FPC-FP520R
VDD3V3
VDD5V
BUFF_DIR
BLT_PWM
BKLGHT_PWM
V_IO=3.3V
Title: ET6ULL BB
Size: A3
Document Number: Cover
Rev: Rev0.0
Draw By: <Drawing>
Date: Friday, March 25, 2022
Sheet: 10 of 14

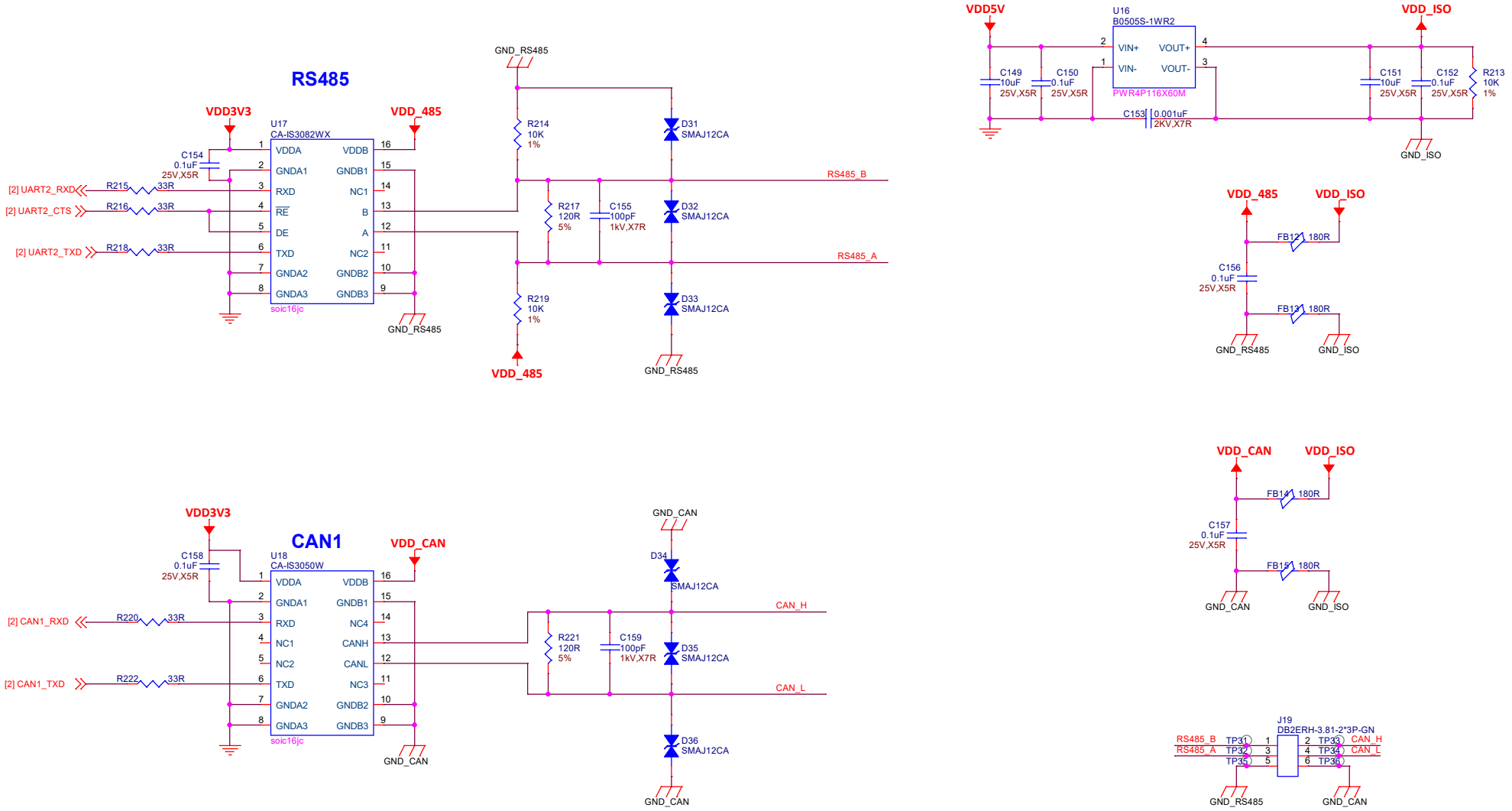
Boot Select



MicroSD

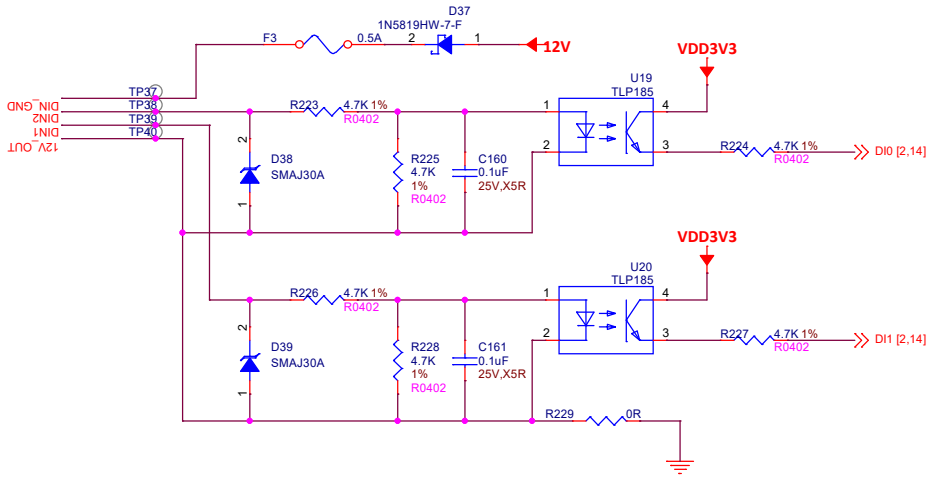


	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Friday, March 25, 2022	Sheet: 11 of 14

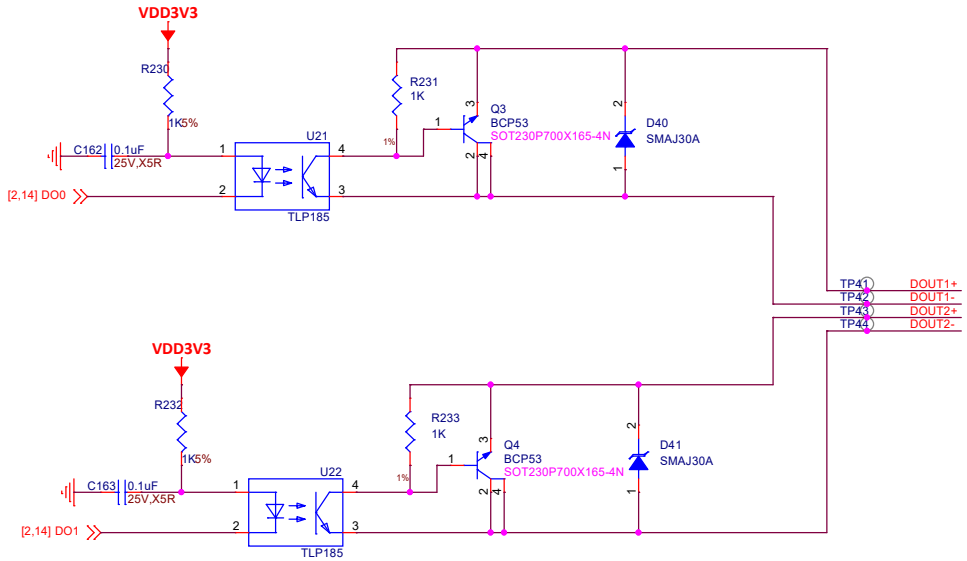


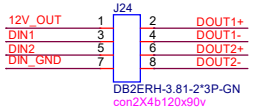
	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Friday, March 25, 2022	Sheet: 12 of 14

DI

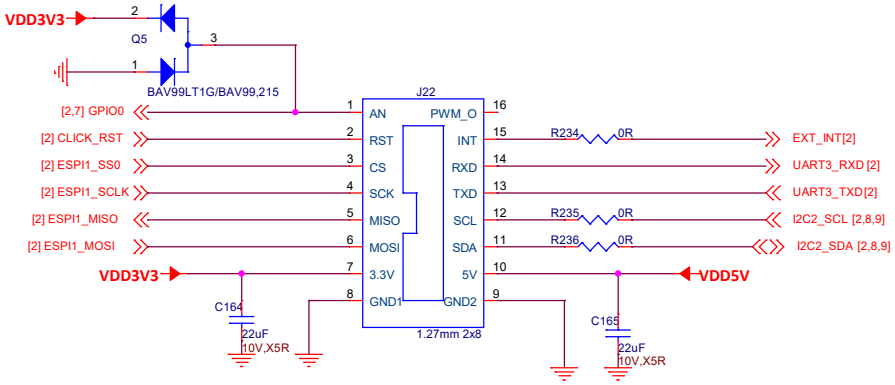


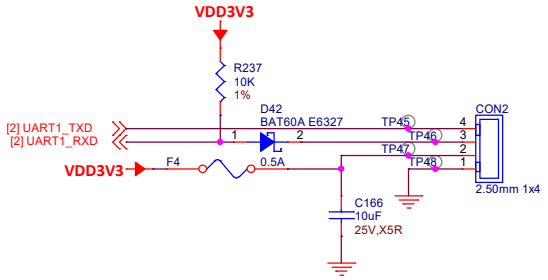
DO

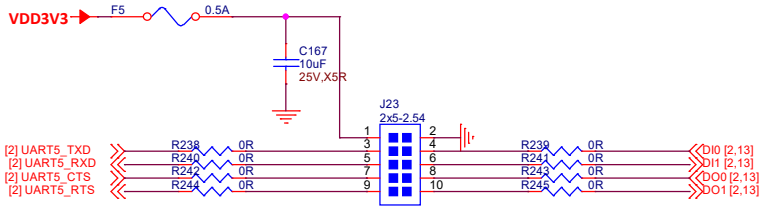




	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Friday, March 25, 2022	Sheet: 13 of 14







	Title: ET6ULL BB	
Size: A3	Document Number: Cover	Rev: Rev0.0
Draw By: <Drawing>	Date: Monday, July 04, 2022	Sheet: 14 of 14