

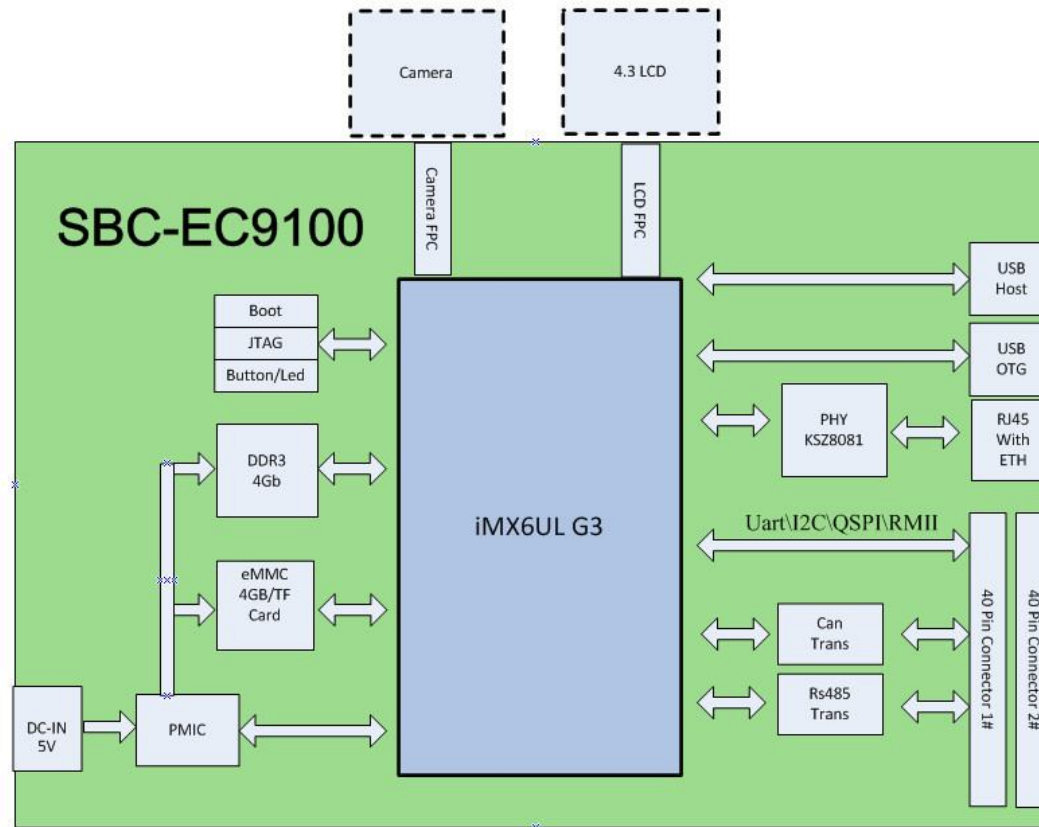
SBC-EC9100

Revision History

DATE	REVISION	DESCRIPTION
31 Dec 2015	SBC-EC9100 Rev 00	
	SBC-EC9100 Rev 01	<ul style="list-style-type: none">- Add Y3\R311\R312\C228,DNP R39\Y2, Modif i edt he U\$B po wer Add D\$ dd C\$ \ C\$- Modif i edt he MD O&MDÇ S vapt he Uart 1 and Uart 3- del lcd_pwr control,need to add the GPIOs control to LCD& WIFI
	SBC-EC9100 Rev 02	<ul style="list-style-type: none">- Changed Rs485 connect i on D\$ RTS si gnd- Add RUN LED- Changed Power out of WIFI model- Changed Reset circuit and SPI2

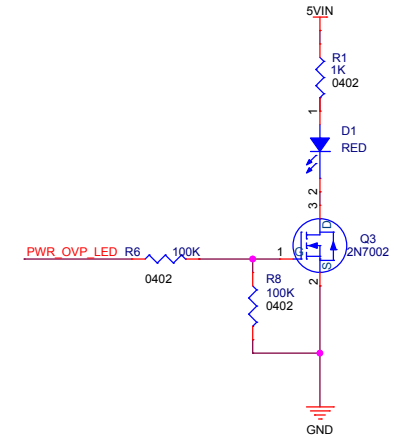
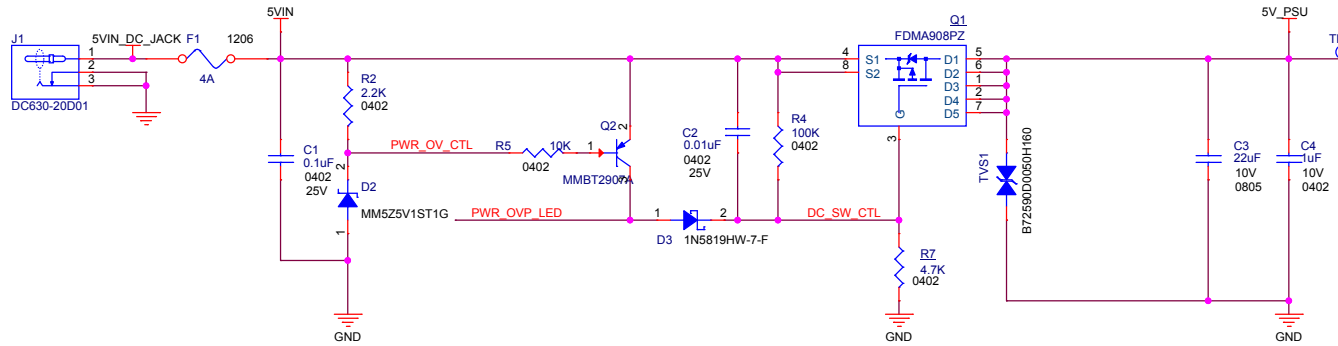
Note : DNP = Do Not Populate

EVK-EC9100 BLOCK DIAGRAM



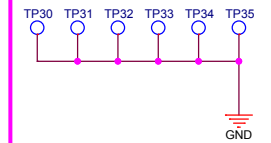
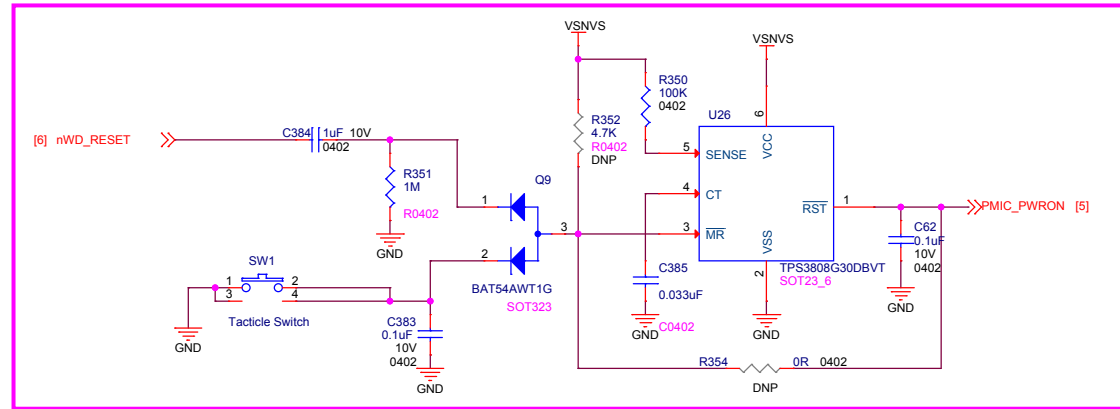
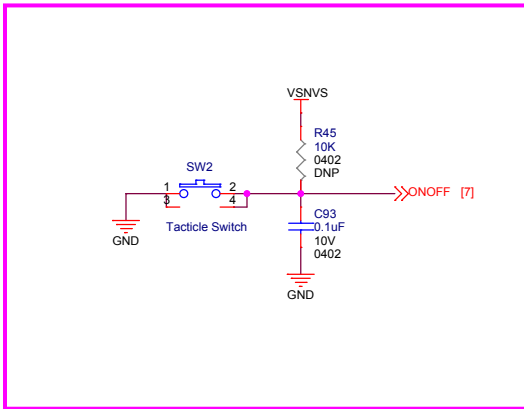
5V DC POWER

OVER VOLTAGE PROTECTION

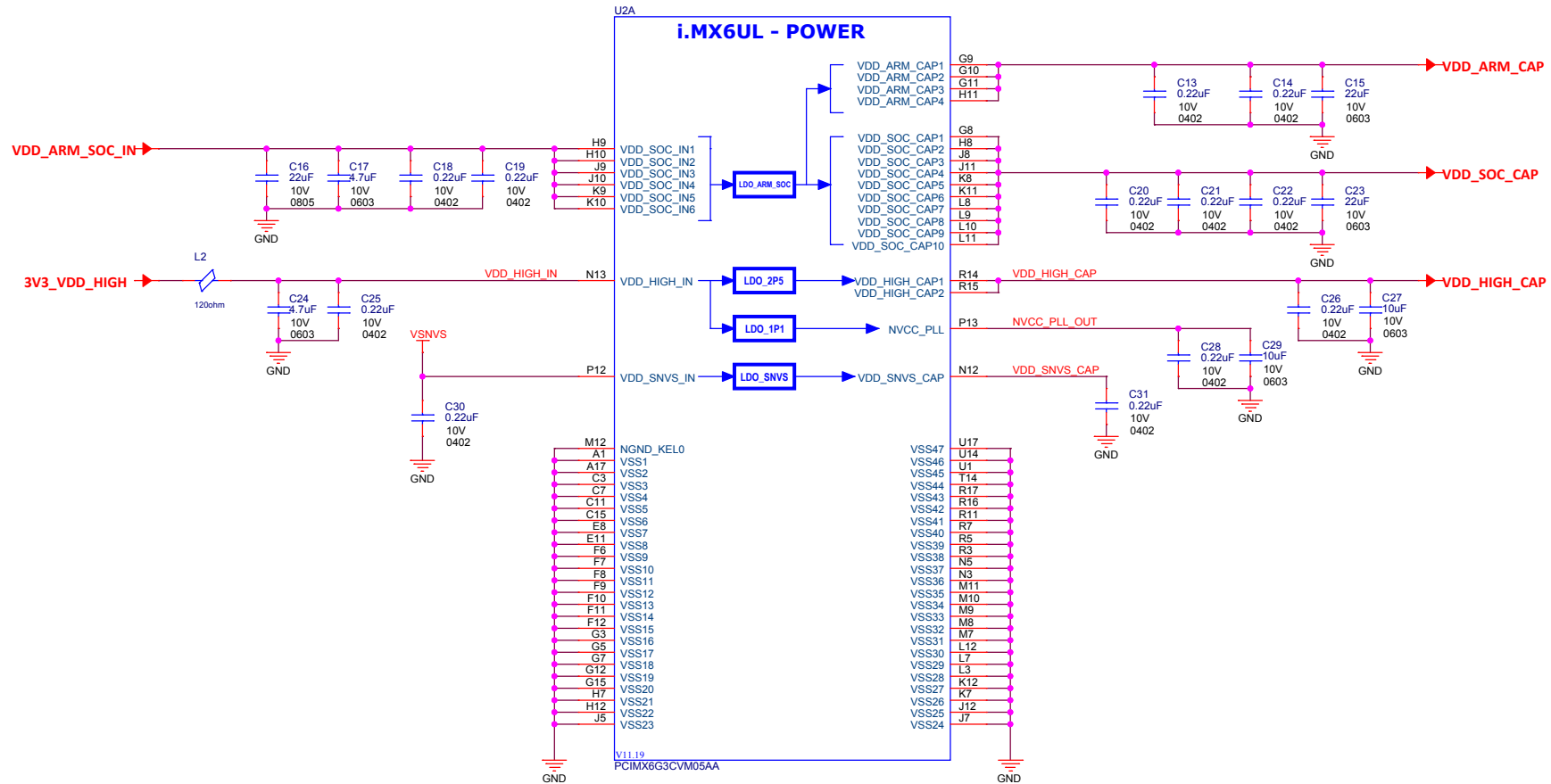


Power ON/OFF

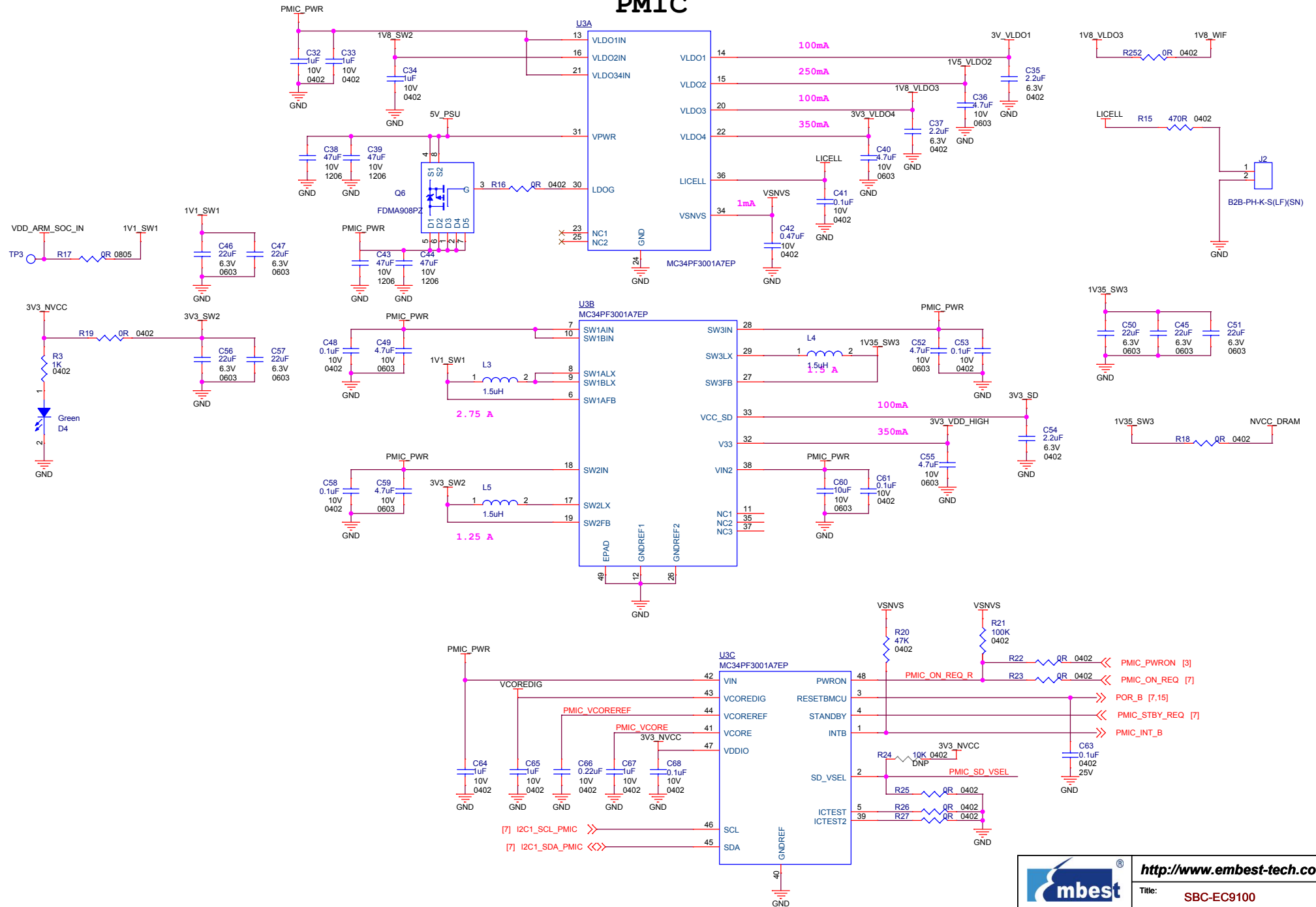
Reset CPU




i.MX6UL PWR

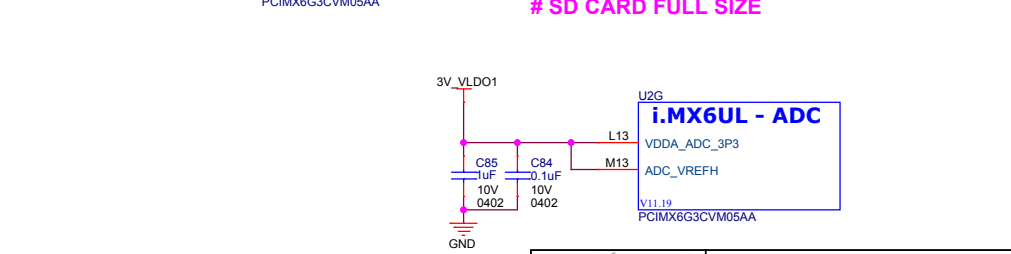
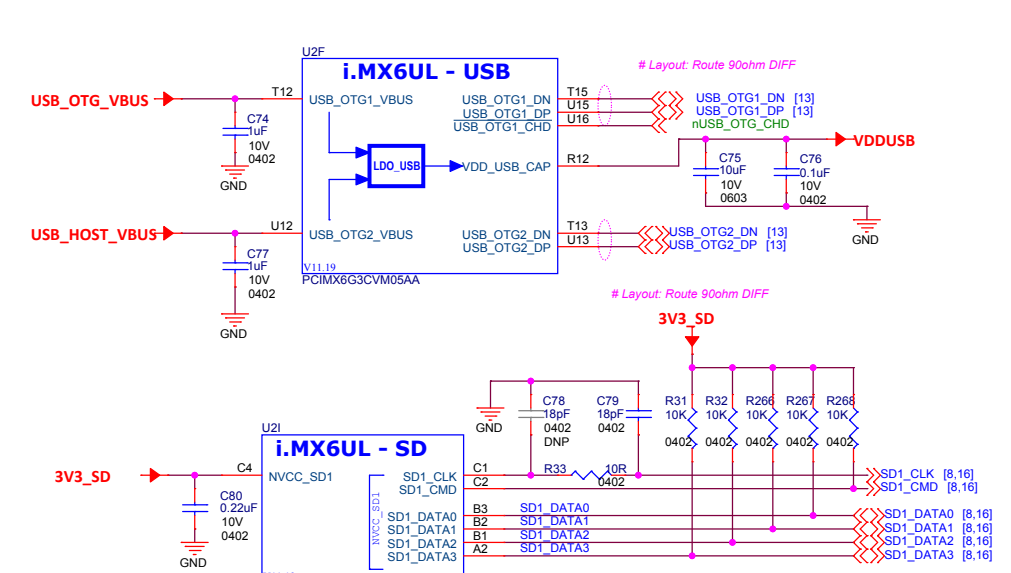
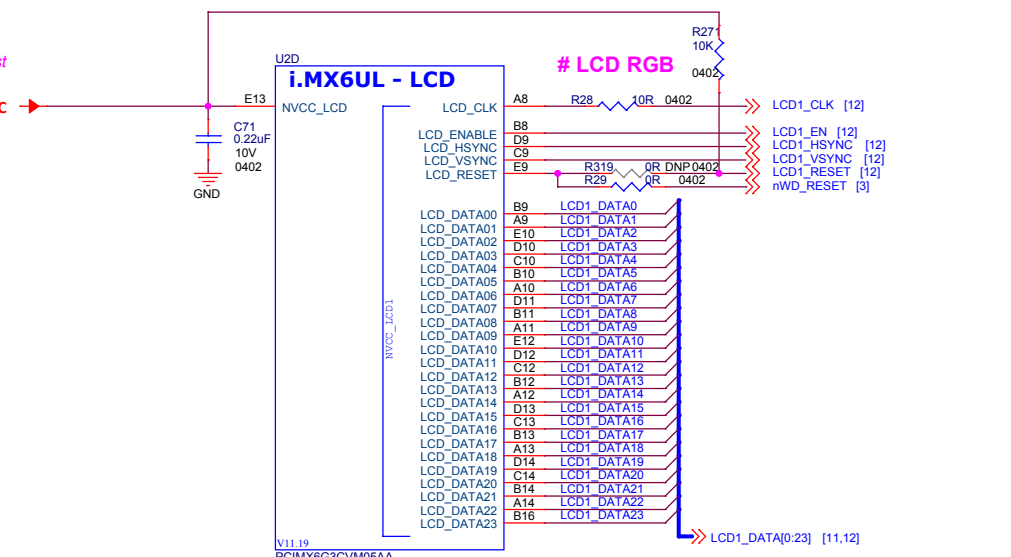
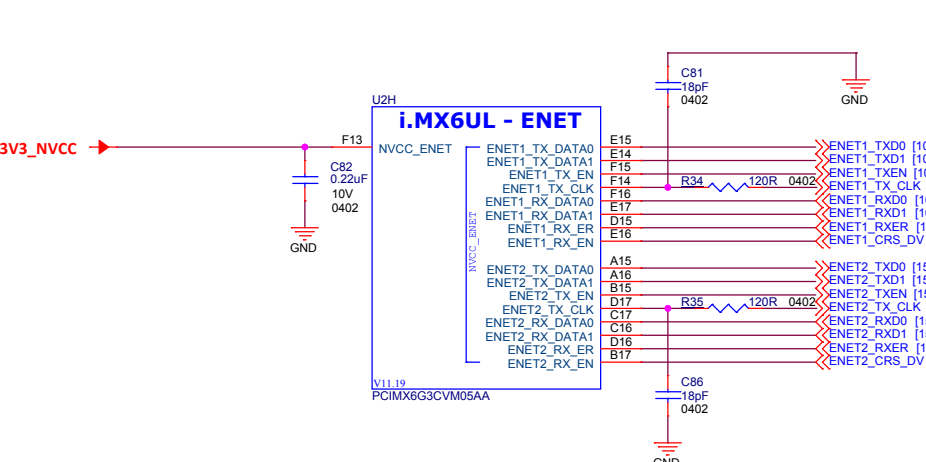
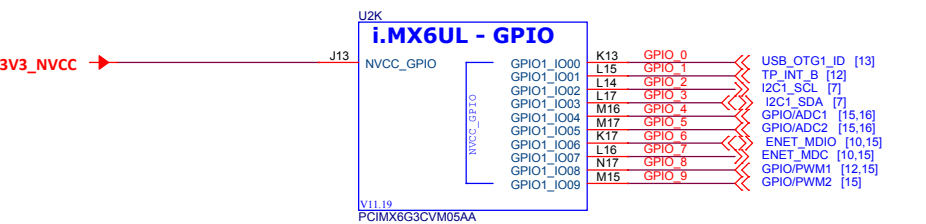
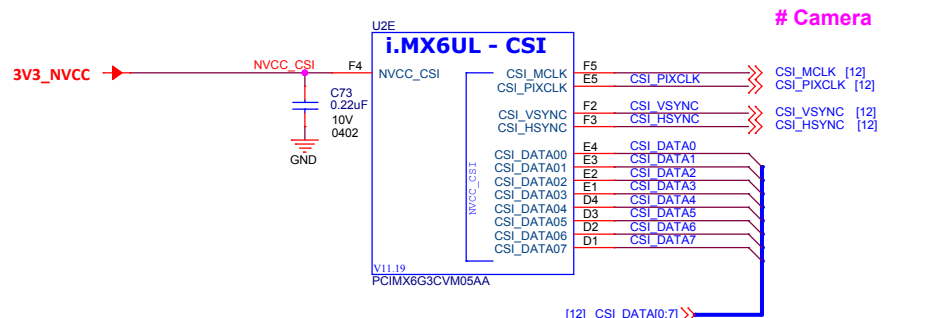
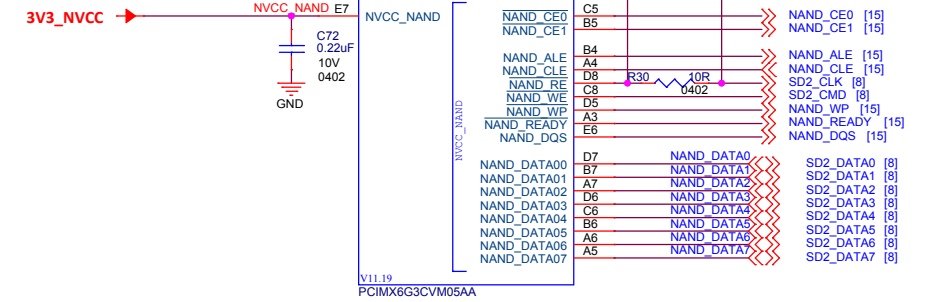


PMIC



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		Title: SBC-EC9100	
Size: A3	Document Number: 05_PMIC	Rev: 01	Draw By: Roy
Date: Tuesday, May 24, 2016		Sheet: 5 of 16	

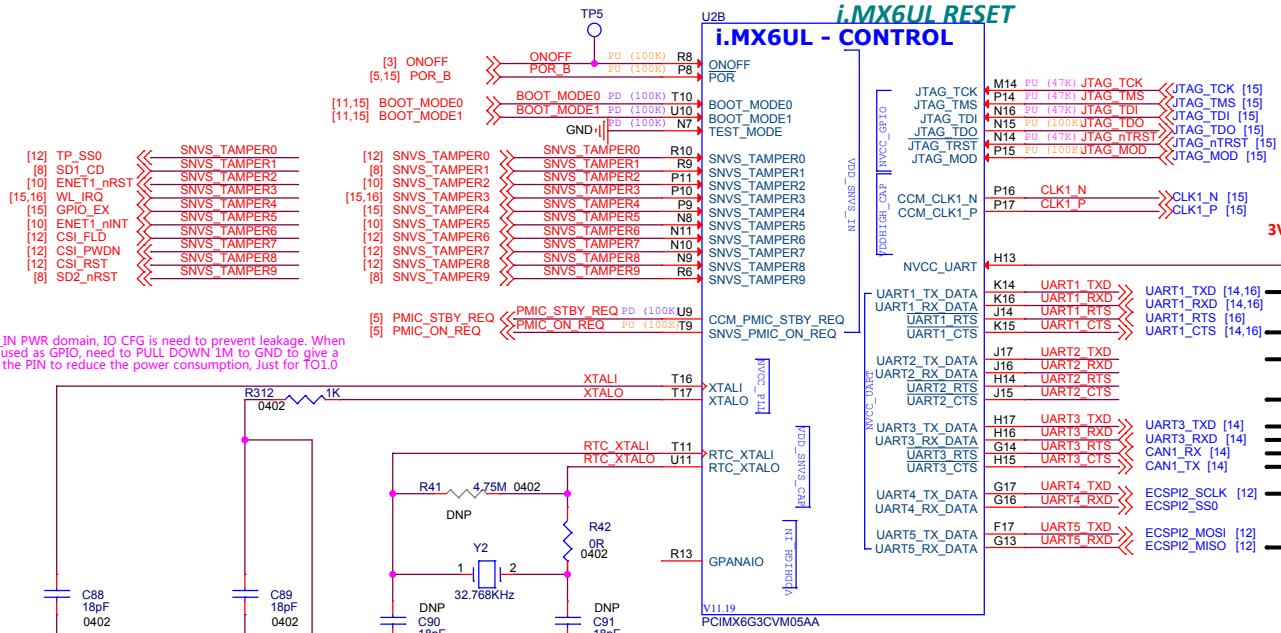
MX6UL PERI



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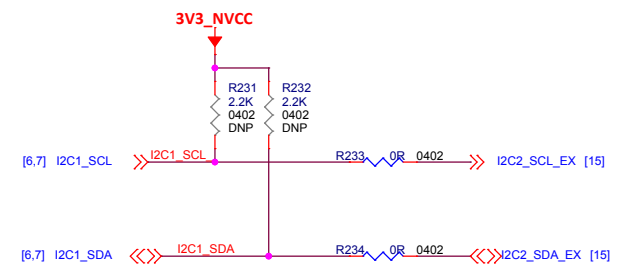
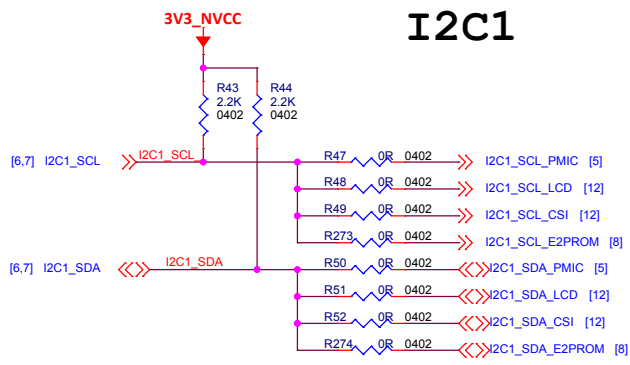
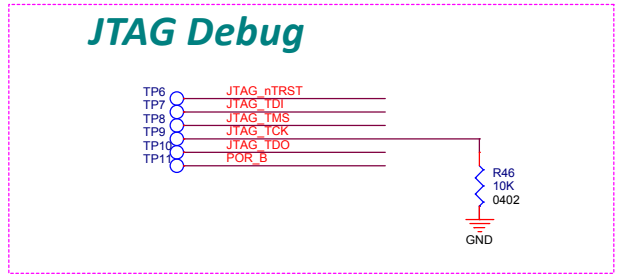
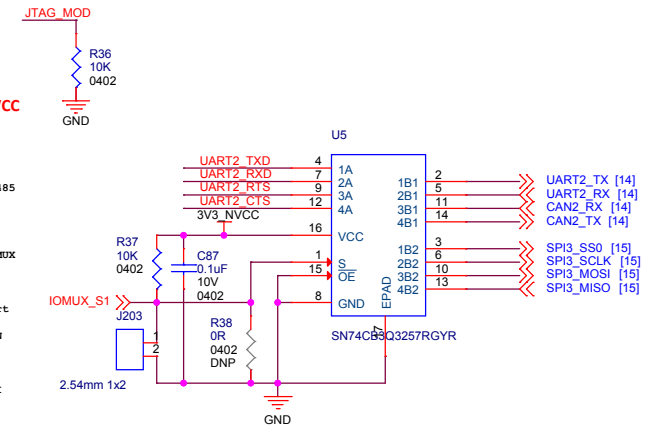
Title: **SBC-EC9100**

Size: A3	Document Number: 06_CPU PERI1	Rev: 01
Draw By: Roy	Date: Tuesday, May 24, 2016	Sheet: 6 of 16



VDD_SNVS_IN PWR domain, IO_CFG is need to prevent leakage. When TAMPER PIN used as GPIO, need to PULL DOWN 1M to GND to give a fixed state to the PIN to reduce the power consumption, Just for TO1.0

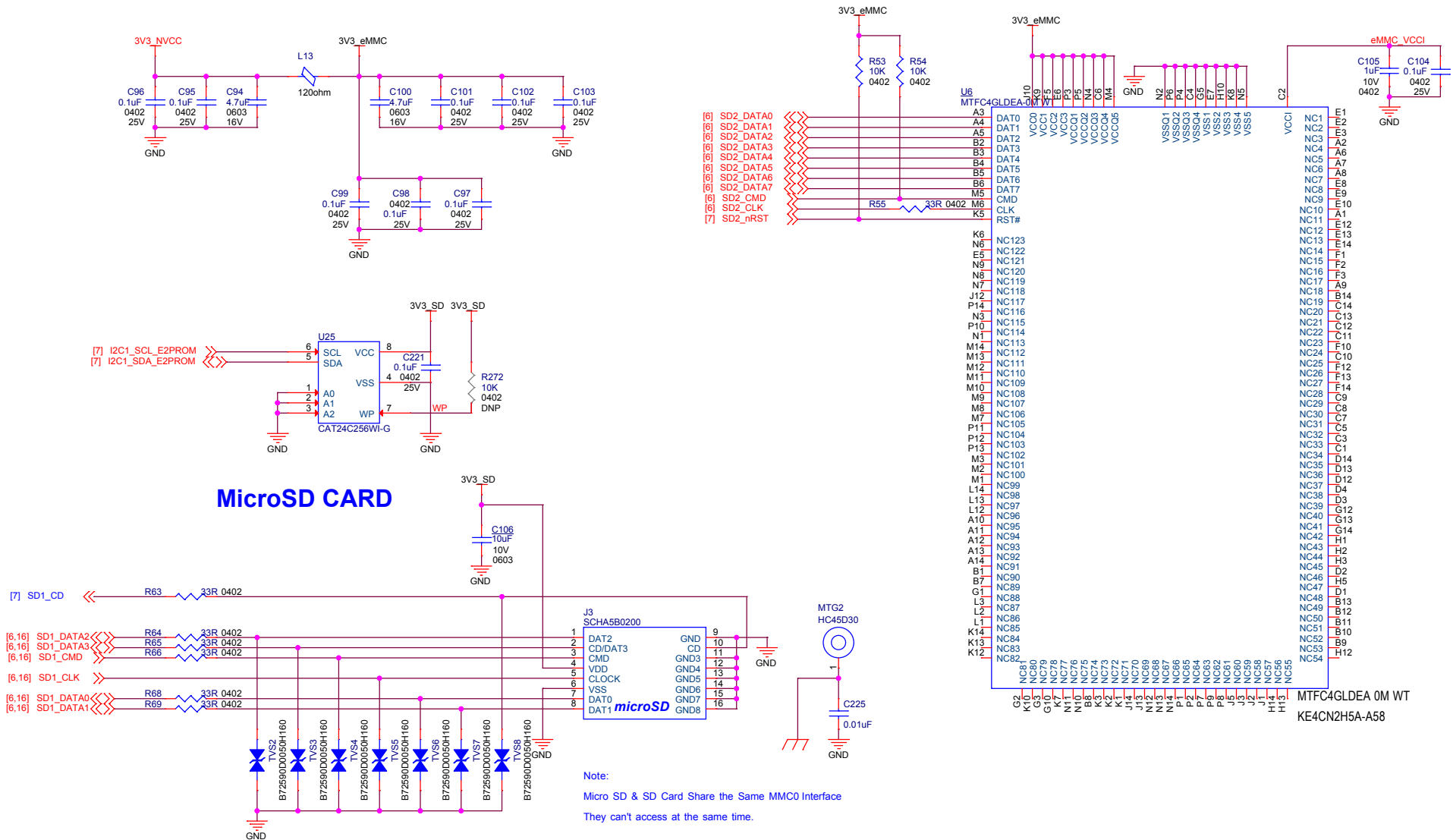
NVCC_GPIO (J13) and NVCC_UART (H13) should share one 0.22uF de-coupling cap. There is no PCB space to fit two caps.

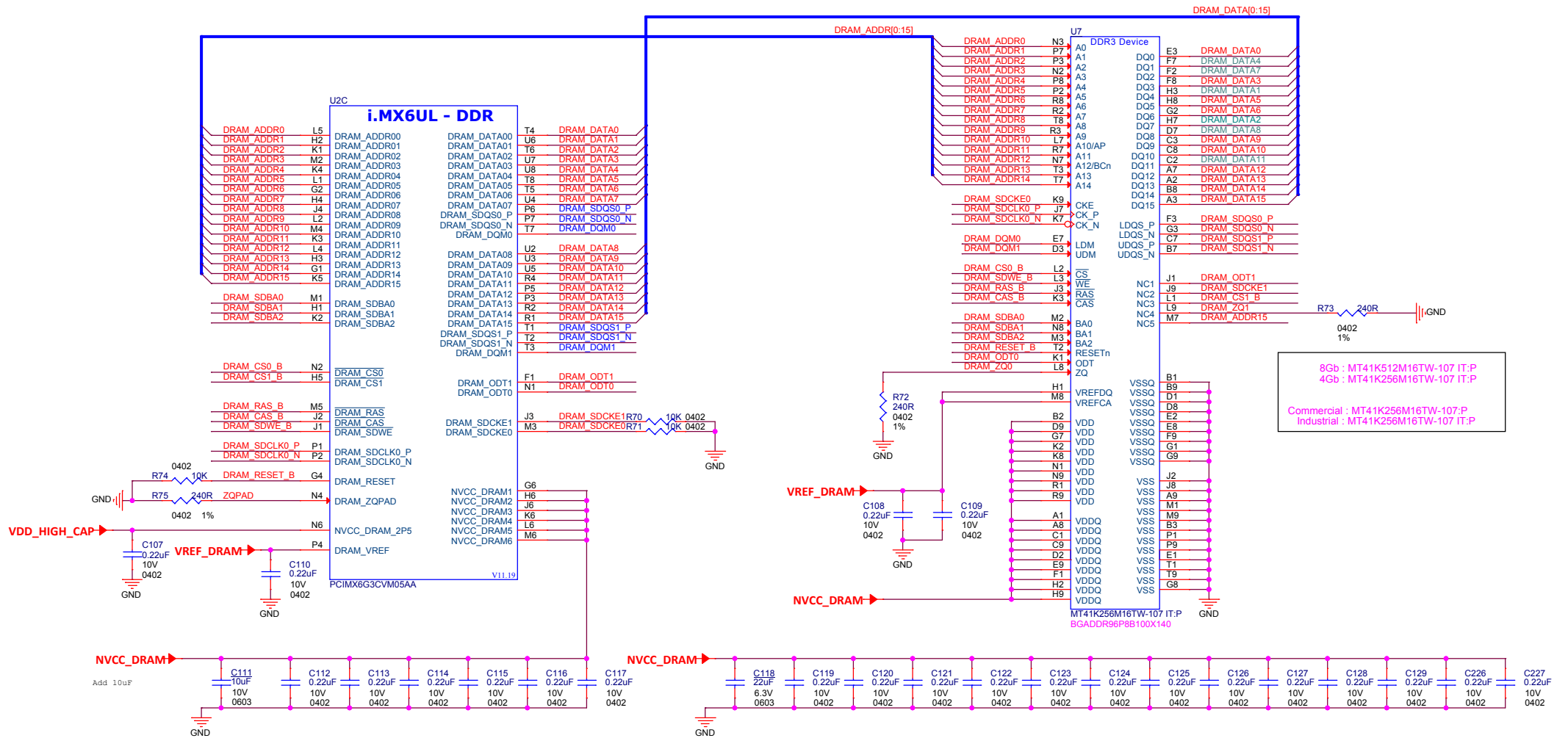


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Size: A3	Document Number: 07_CPU PER12	Rev: 01	
Draw By: Roy	Date: Thursday, May 26, 2016	Sheet: 7 of 16	

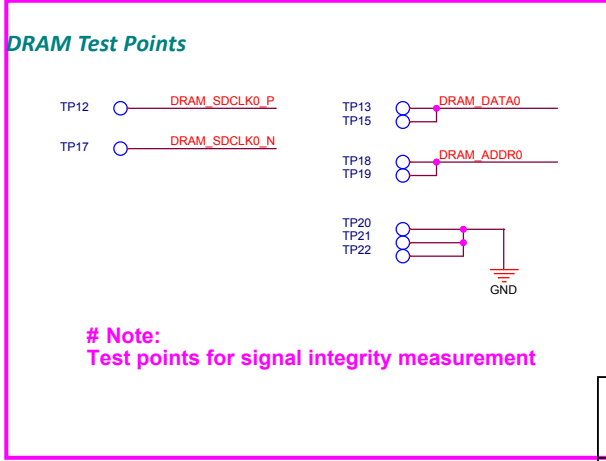
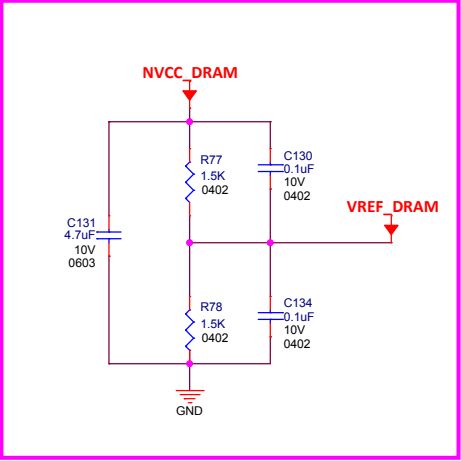
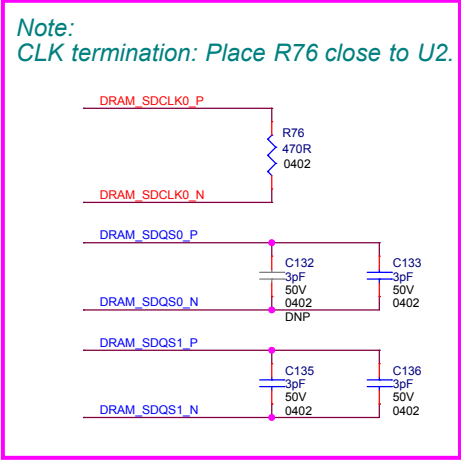
eMMC Storage <4.51>

Option 2

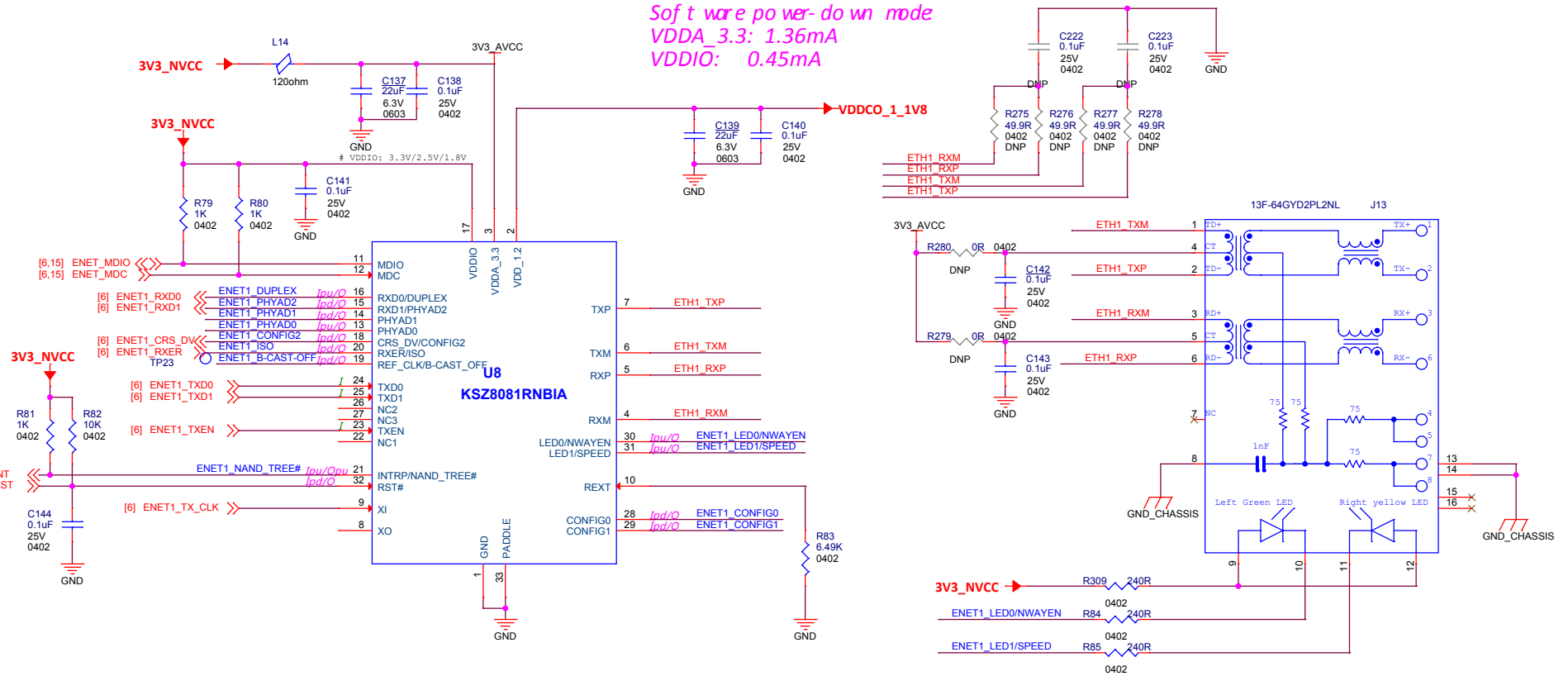




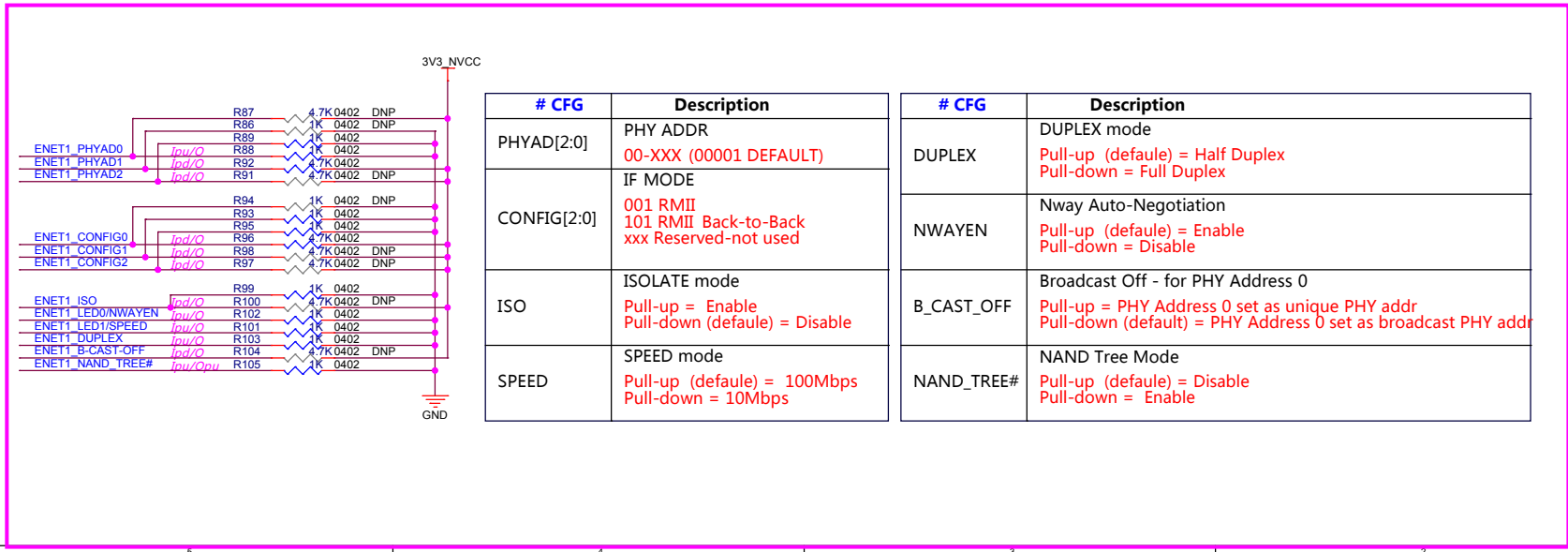
8Gb : MT41K512M16TW-107 IT-P
 4Gb : MT41K256M16TW-107 IT-P
 Commercial : MT41K256M16TW-107-P
 Industrial : MT41K256M16TW-107 IT-P



Software power-down mode
 VDDA_3.3: 1.36mA
 VDDIO: 0.45mA



RMII CFG



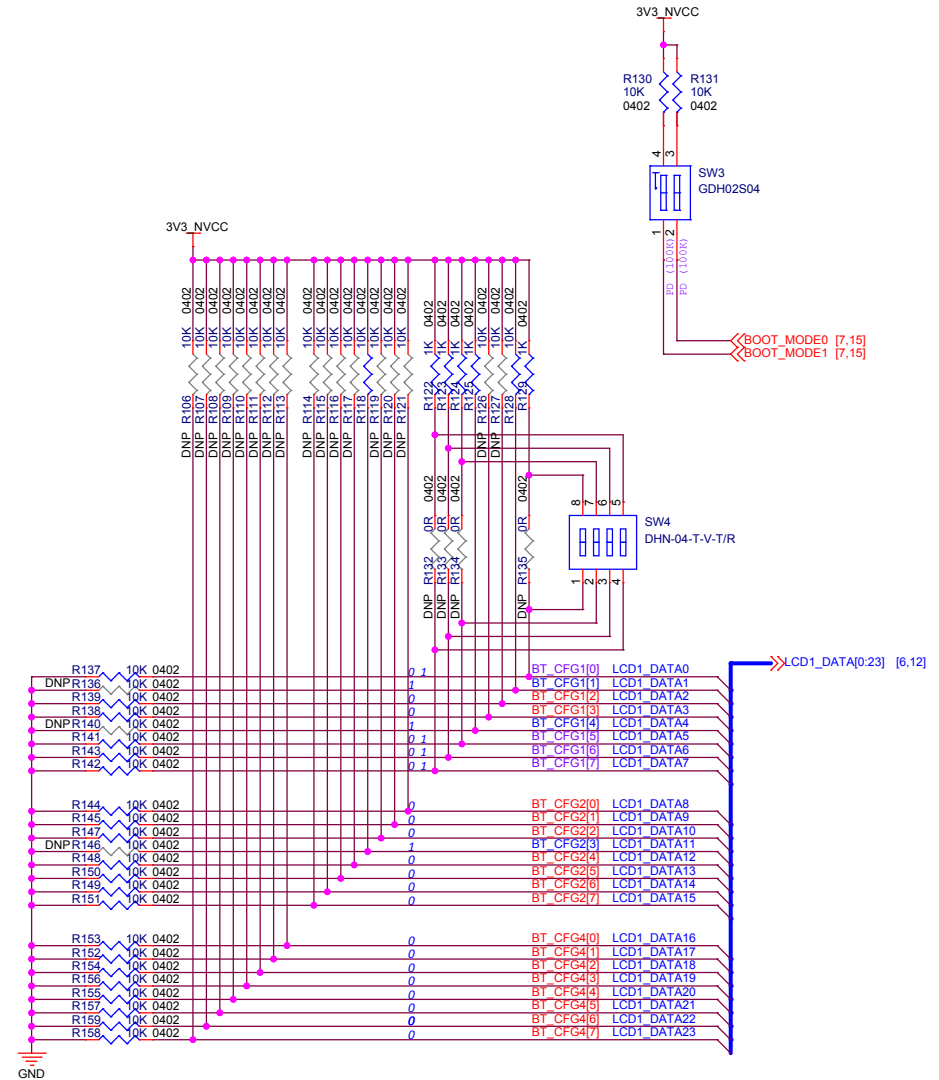
FUSE MAP

Boot Configuration

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
QSPI	0	0	0	1	Reserved		DDSRMP: "000": Default "001-111"	
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	SD Power Cycle Enable 0 - No power cycle 1 - Enabled via USDHC_RST pad (USDHC3 & 4 only)	SD Loopback Clock Source: Self/for SDR50 and SDR104 only 0 - through SD pad 1 - direct	
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable: 0 - No power cycle 1 - Enabled via USDHC_RST pad (USDHC3 & 4 only)	SD Loopback Clock Source: Self/for SDR50 and SDR104 only 0 - through SD pad 1 - direct
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address.bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
QSPI	Reserved	HSPHS: Half Speed Phase Select 1 on 0: select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay select 1 on 0: one clock delay 1: two clock delay	FSPHS: Full Speed Phase Select 1 on 0: select sampling at non-inverted clock 1: select sampling at inverted clock	FSLDLY: Full Speed Delay select 1 on 0: one clock delay 1: two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16 01 - A+DH 10 - A+DL 11 - Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibrat i on Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11 - Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SD1 VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles.		BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 12ms '1' - 22ms (LBA Nand)	Reserved

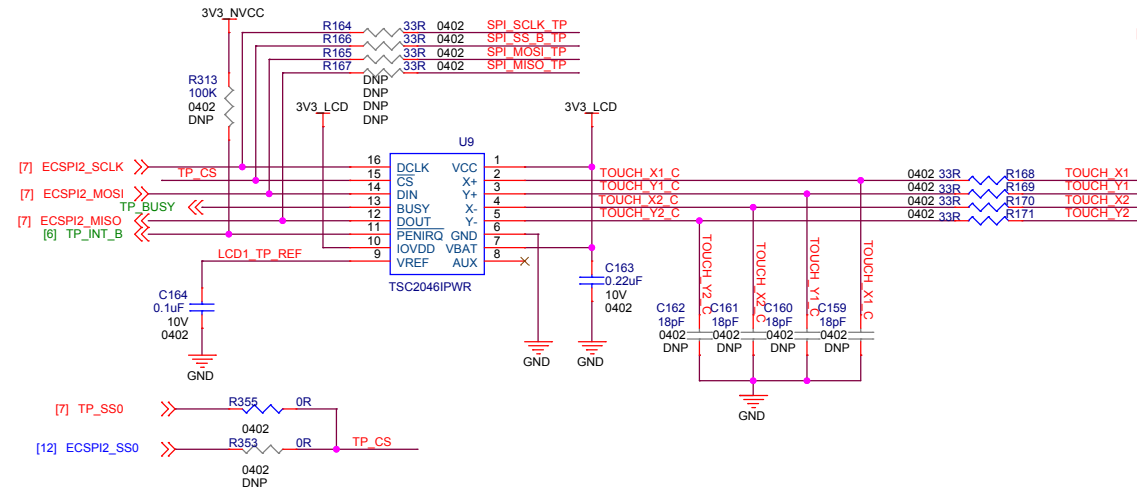
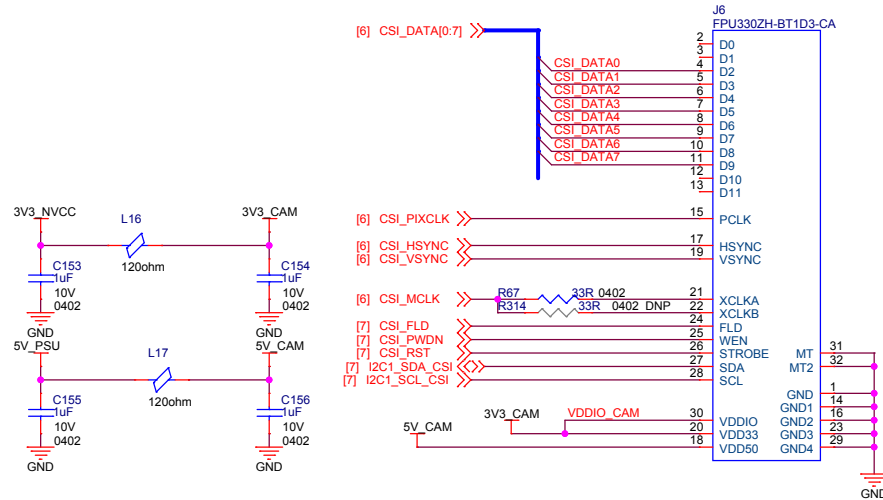


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 Title: **SBC-EC9100**
 Size: A3 Document Number: 11_Boot_CFG Rev: 01
 Draw By: Roy Date: Monday, May 23, 2016 Sheet: 11 of 16

Camera

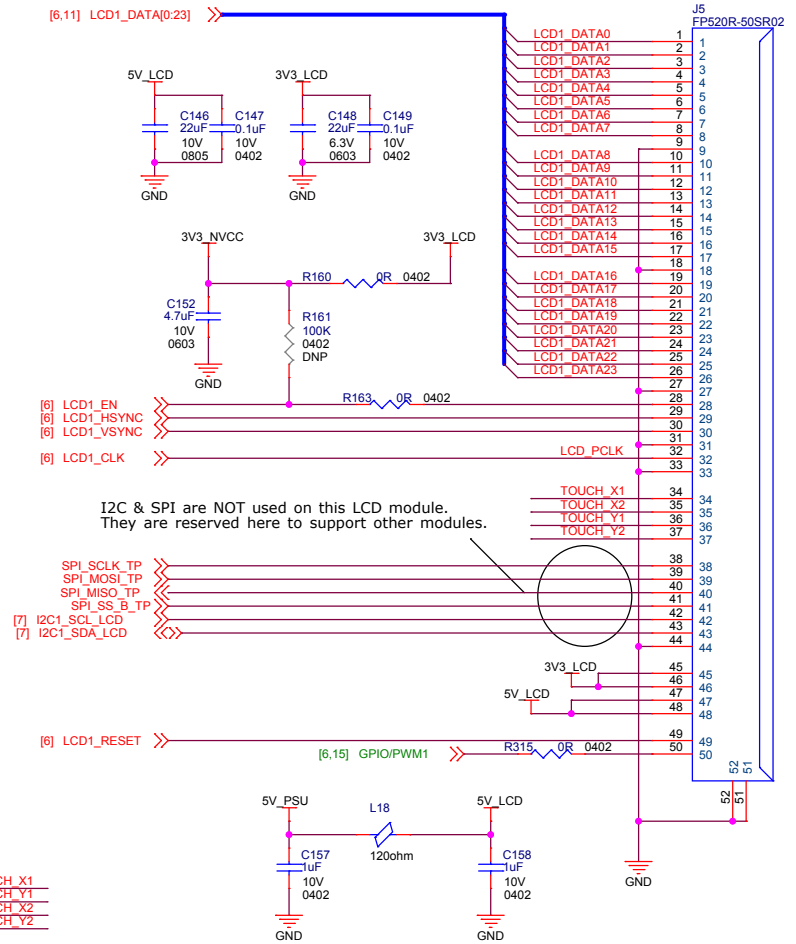
Note: All GPIO use 3.3V

Compatible 10bit camera

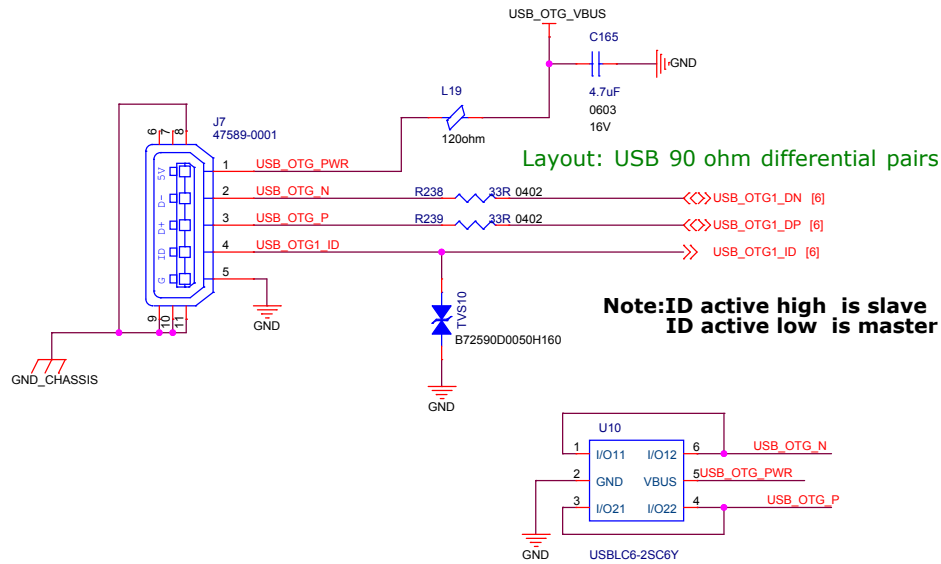


LCD

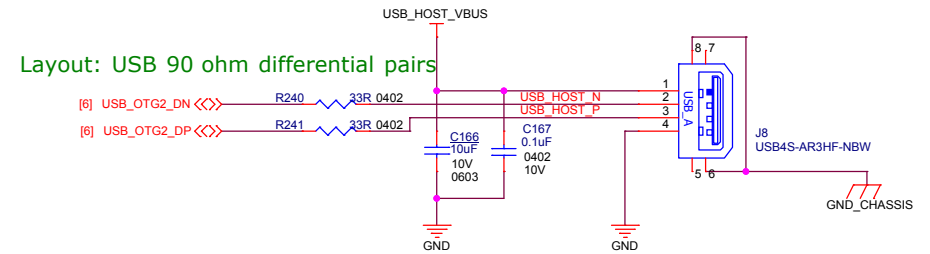
LCD8000-43T from Embest



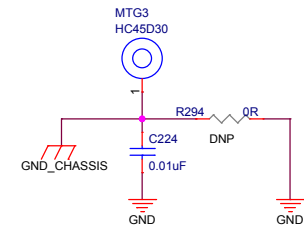
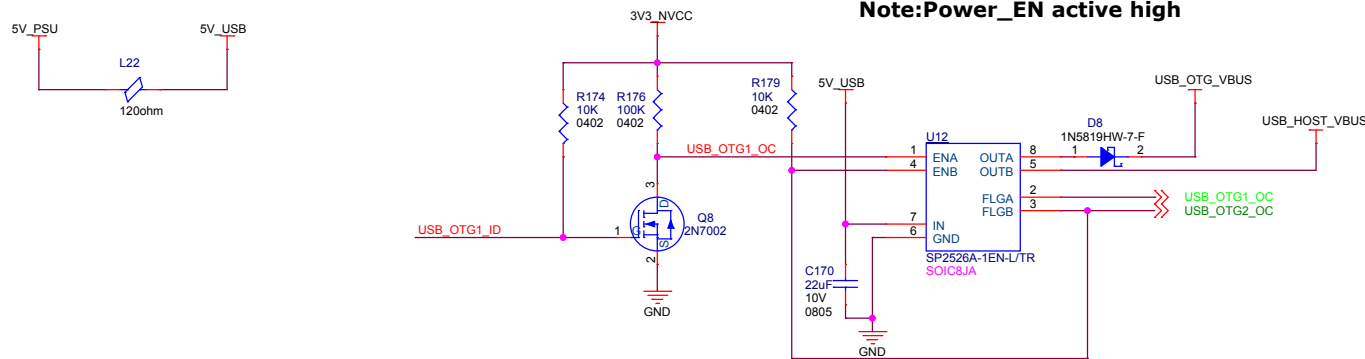
USB OTG



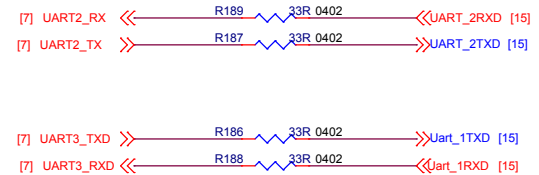
USB HOST



USB Power

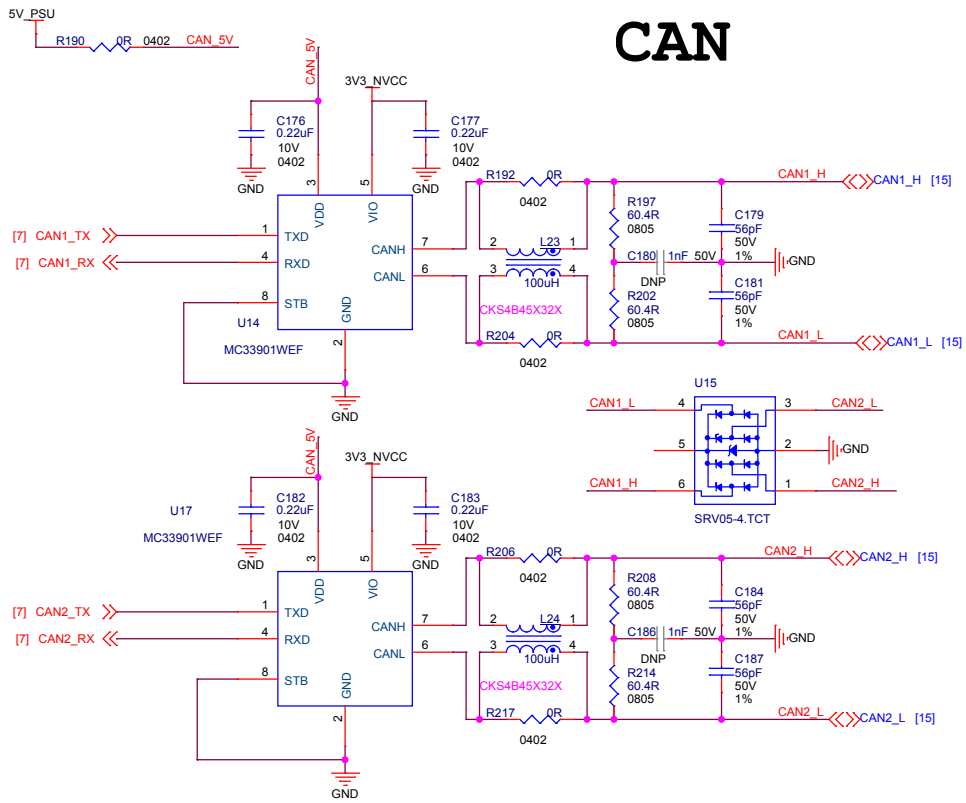


RS232 (TTL)

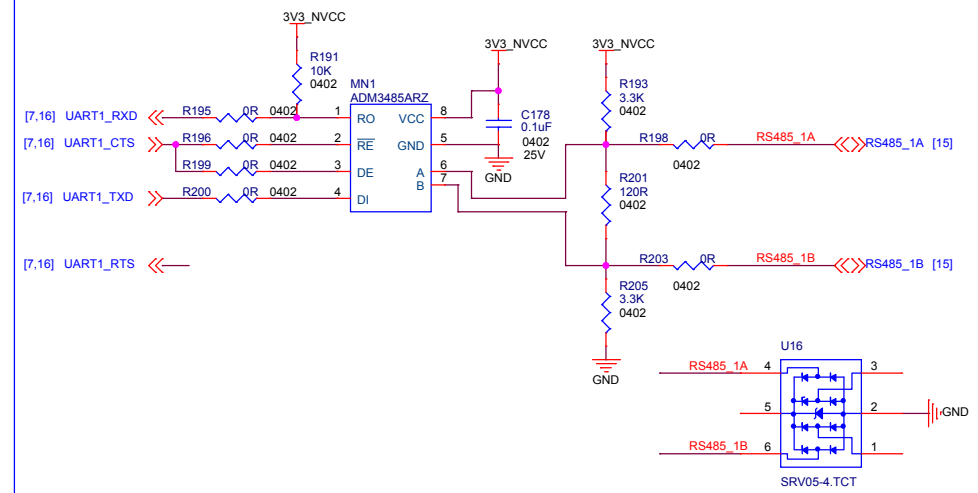


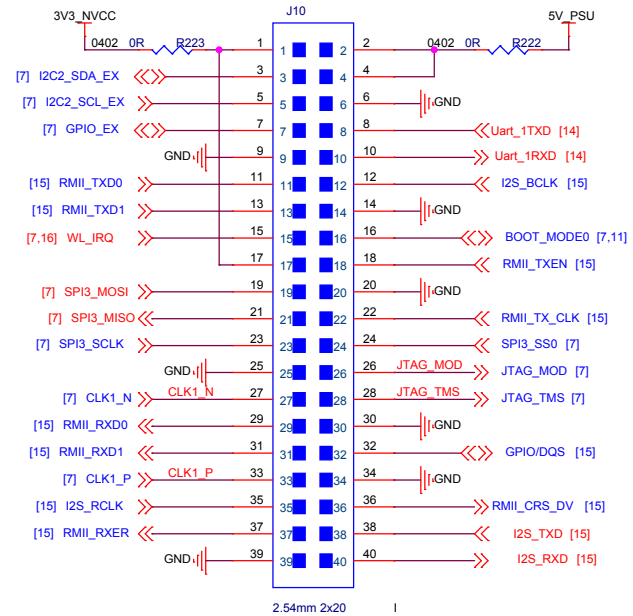
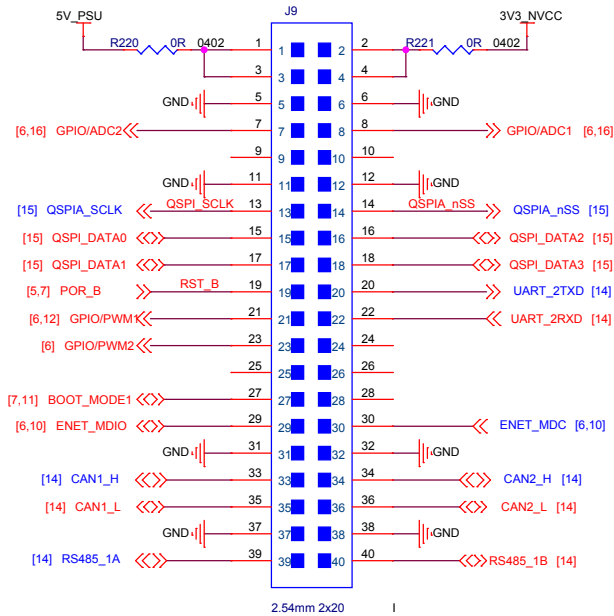
Debug

CAN

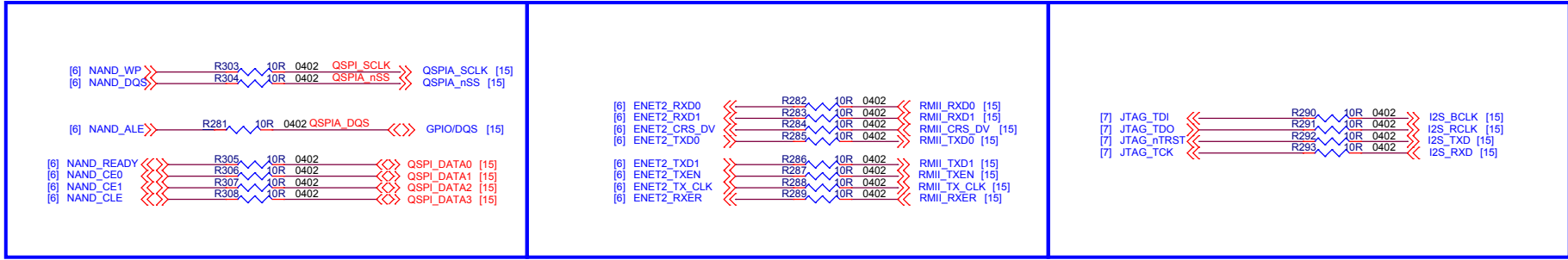


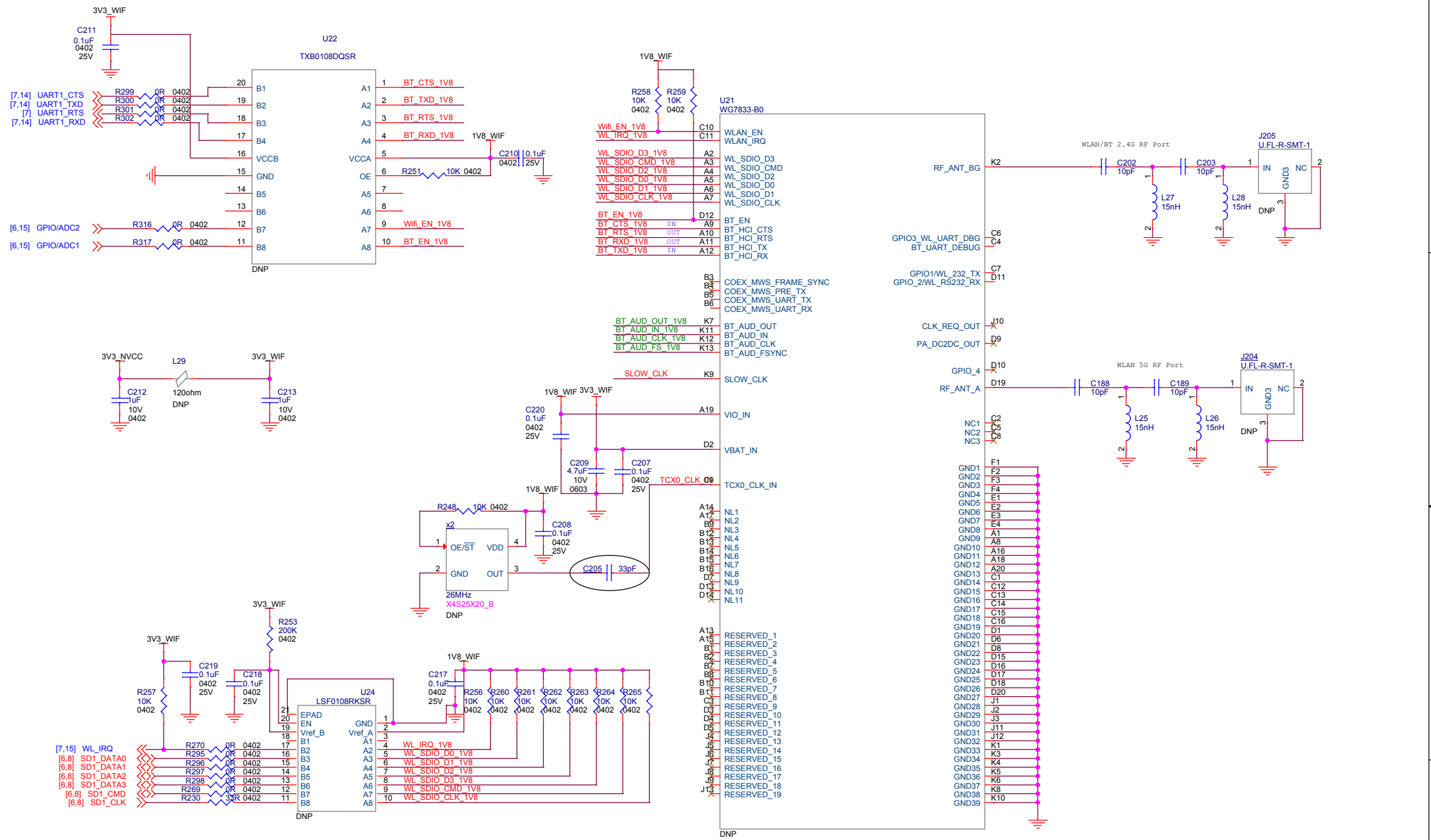
RS485






Debug





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		Title: SBC-EC9100	
Size: A3	Document Number: 16_Wifi_BT	Rev: 01	
Draw By: Roy	Date: Tuesday, May 24, 2016	Sheet: 16 of 16	