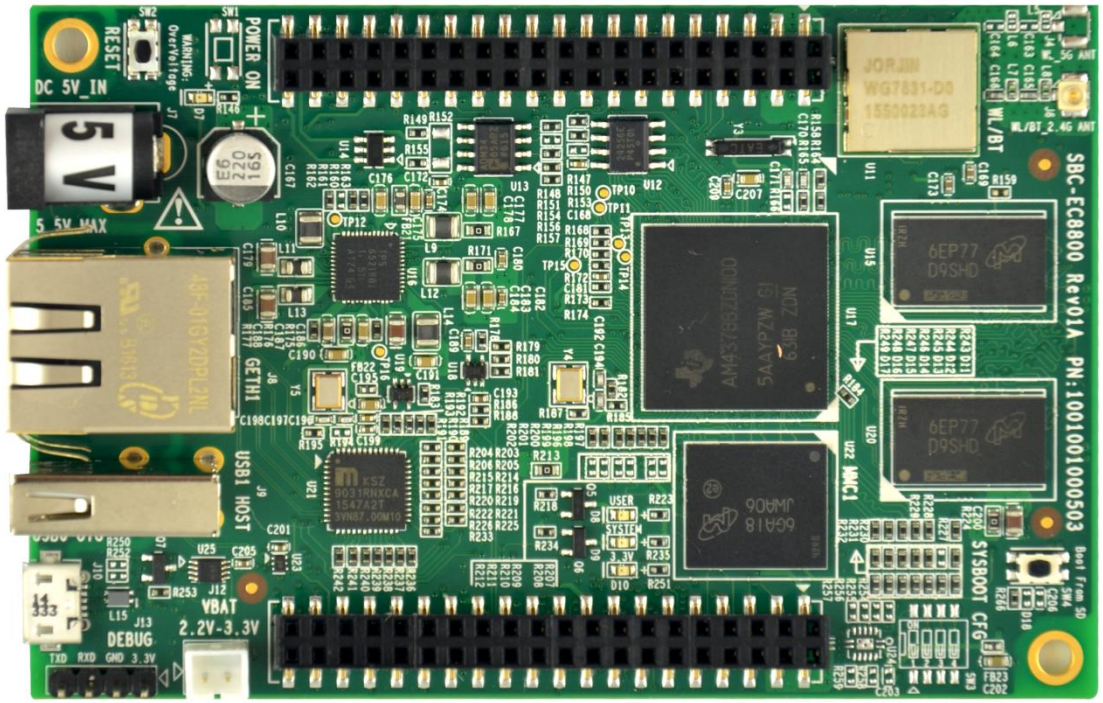
User Manual

[SBC-EC8800]



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Compliance Information:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-- Reorient or relocate the receiving antenna.

-- Increase the separation between the equipment and receiver.

-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-- Consult the dealer or an experienced radio/TV technician for help.

History

Rev.	Note	Author
Rev1.0	Initial	John Xin
Rev1.1	Changed the description of WLAN	John Xin

Catalog

Chapter 1 Product Overview

1.1 Brief Introduction

SBC-EC8800 is designed by Embest Technology Co., Ltd, targeting on medical instruments, industrial control, communications and other fields launched an evaluation board based on TI AM437x. This processor integrates up to 1GHz ARM Cortex™-A9 core and provides rich peripheral interfaces. SBC-EC8800 can provide a series of expansion peripheral interfaces, including one network interface, one USB 2.0 Host interface and one USB 2.0 OTG interface, one debug UART interface, one TFT screen and resistive touch screen interface, one camera interface, one MicroSD card interface, one WLAN+Bluetooth interface. In addition, from the expansion headers, there are a number of other signals including one RS485, two CAN, two I2C, two UART, one RGMII, one SPI, one MCASP, four ADC, three PWM and two GPIO etc.

SBC-EC8800 has a very wide range of application scenarios to meet, including gaming peripherals, home and industrial automation, consumer medical devices, printers, intelligent charging system, intelligent vending machines, weighing system, terminal education, toys, and so on, in all areas of different needs.

1.1.1 Packing List

- SBC-EC8800 Evaluation Board X1
- Desiccant X1
- Antistatic Bag X1
- Generic Safety Leaflet X1
- Quick Start Guide X1
- Packing Box X1

1.1.2 Product Features

- **Electrical Features**
  - Operating Temperature: 0~70°C（Commercial）, -40~85°C（Industrial）
  - Power Supply: 5V/2A (The power adapter with short circuit current limit)
  - Operating Humidity: 20% ~ 90%（no condensation）
  - Main Board Size: 100 mm × 65 mm
  - PCB Specification: 8 layer design
- **Processor Features**
  - 1000 MHz ARM Cortex™-A9 32-Bit RISC Microprocessor
  - SGX530 Graphics Engine

- Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)
- Real-Time Clock (RTC)

- **Onboard Hardware Features:**
  - 1GB DDR3 SDRAM
  - 4GB eMMC Flash
  - 32KB EEPROM
  - 32MB QSPI Flash
  - Three LED, one is power LED, the other two are user LED
  - One Gigabit Ethernet interface, RJ45 terminal
  - One USB 2.0 Host interface, one USB 2.0 OTG interface
  - One TFT screen and resistive touch screen
  - One camera interface
  - One MicroSD card interface
  - One debug UART
  - Three buttons, one of which is power button, one is reset button, and one is boot button
  - One WLAN+Bluetooth interface
  - With two 40Pin 2.54mm pitch connectors（including one RS485, two CAN, two I2C, two UART, one RGMII, one SPI, one MCASP, four ADC, three PWM and two GPIO etc.）

1.2 Board Component Locations

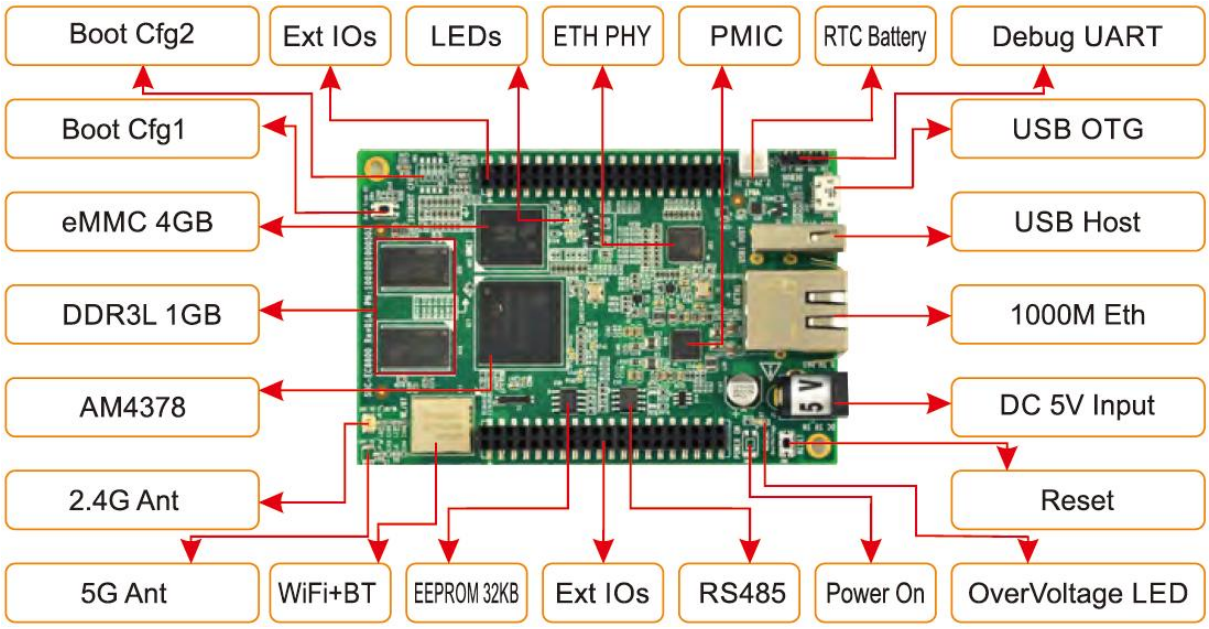


Figure 1-1. SBC-EC8800 Top

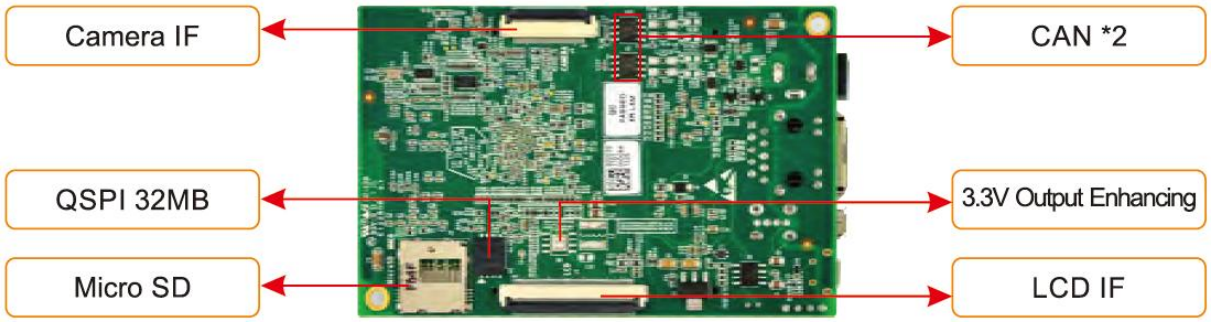


Figure 1-2. SBC-EC8800 Bottom

1.3 System Block Diagram

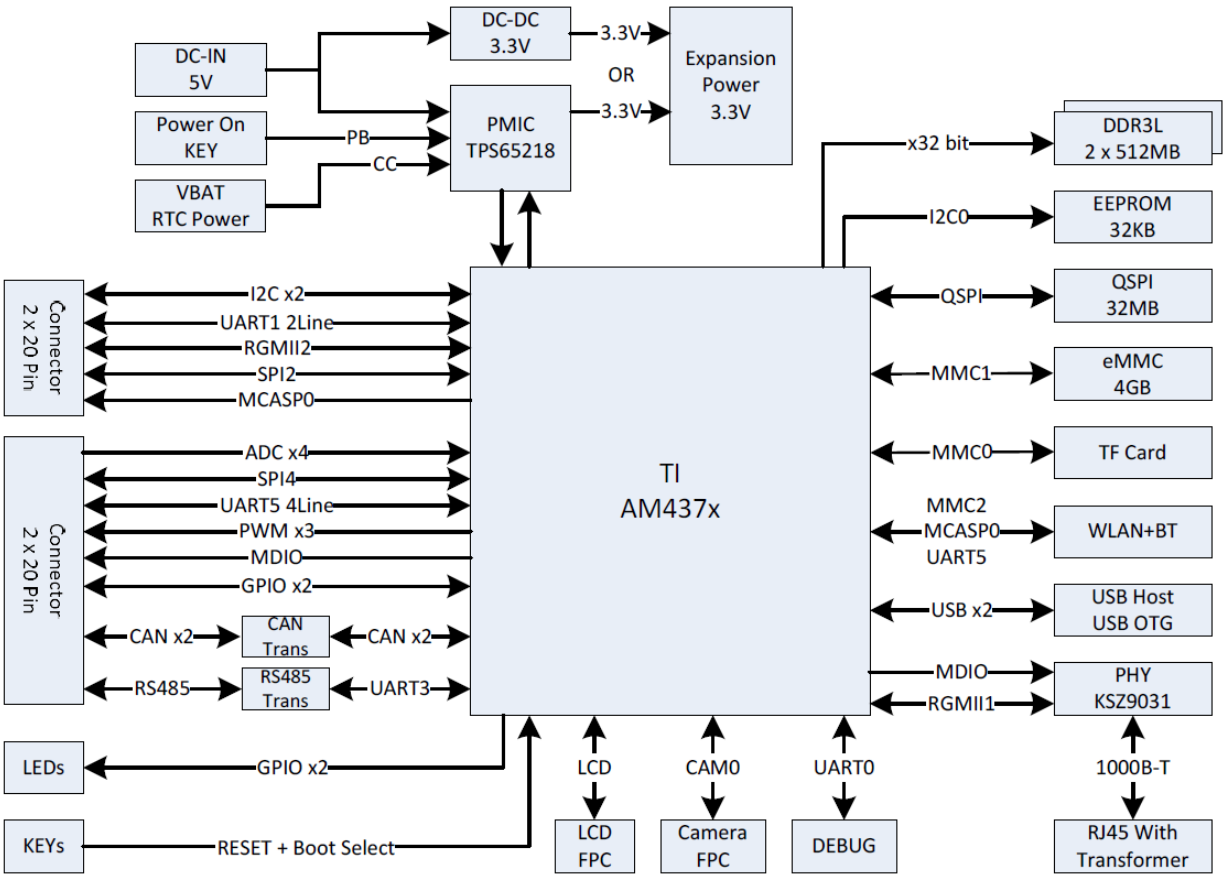


Figure 1-3. SBC-EC8800 System Block Diagram

1.4 Product Dimensions (unit: mm)

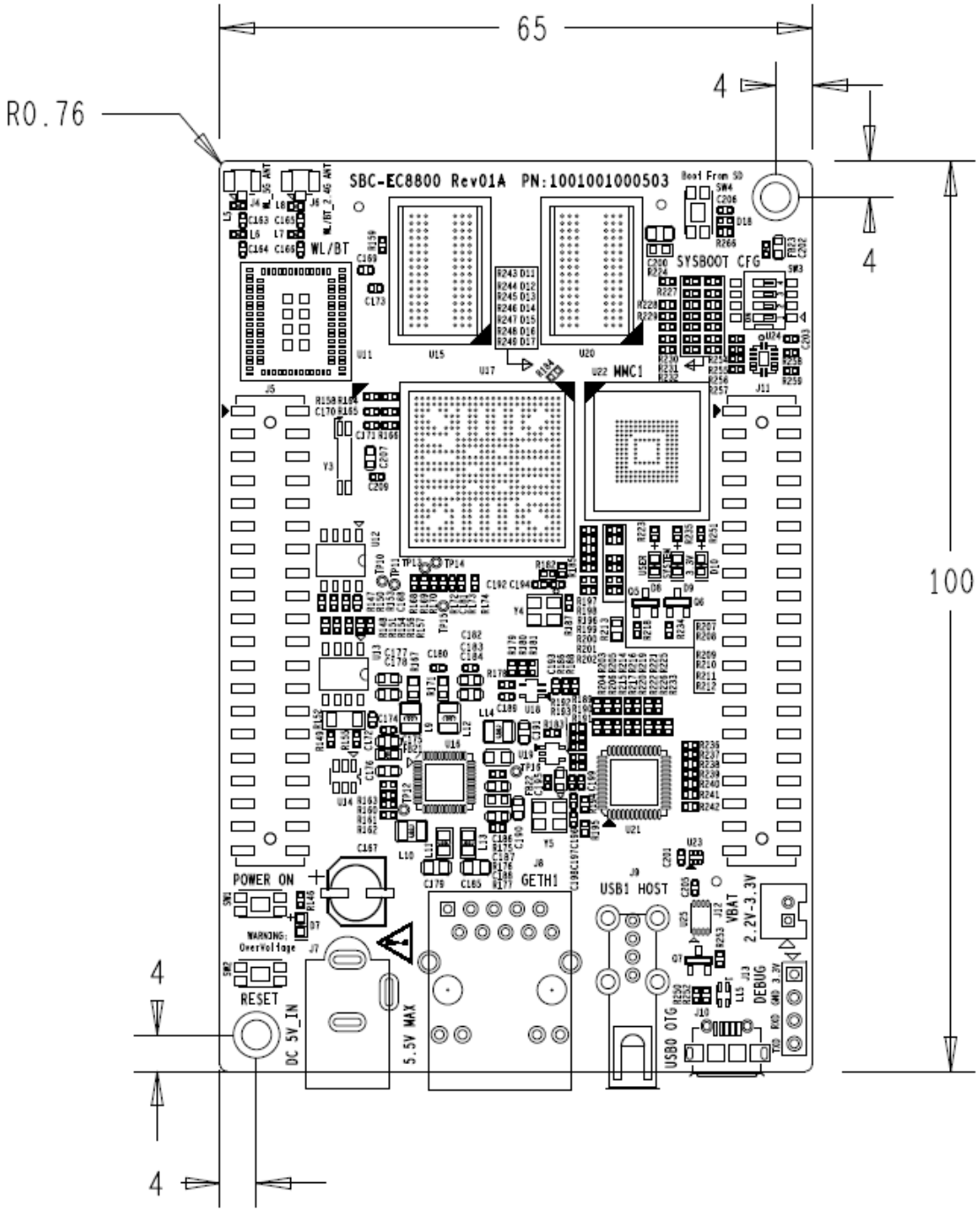


Figure 1-4. Product Dimensions

Chapter 2 Introduction to Hardware System

This chapter will introduce the structure, expansion and peripheral interfaces of SBC-EC8800 hardware system in detail.

2.1 Minimum System

The minimum unit of hardware system is generally composed of CPU, Memory and Management Power. SBC-EC8800 is no exception, and this section mainly introduces the three parts.

2.1.1 CPU

The SBC-EC8800 uses the AM4378 from TI as the CPU and AM4378 is a member of TI AM437x series. The series of high performance processor based on ARM Cortex™-A9 core.

The processors are enhanced with 3D graphics acceleration for rich graphical user interfaces, as well as a coprocessor for deterministic, real-time processing including industrial communication protocols, such as EtherCAT, PROFIBUS, EnDat, and others.

These devices offer an upgrade to systems based on lower performance ARM cores and provide updated peripherals, including memory options such as QSPI-NOR and LPDDR2.

The processors contain the subsystems shown in **Figure 2-1**, and a brief description of each follows.

The processor subsystem is based on the ARM Cortex™-A9 core, and the POWERVR SGX™ graphics accelerator subsystem provides 3D graphics acceleration to support display and advanced user interfaces.

The programmable real-time unit subsystem and industrial communication subsystem (PRU-ICSS) is separate from the ARM core and allows independent operation and clocking for greater efficiency and flexibility. The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos, EnDat, and others. The PRU-ICSS enables EnDat and another industrial communication protocol in parallel. Additionally, the programmable nature of the PRU-ICSS, along with their access to pins, events and all system-on-chip (SoC) resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in off-loading tasks from the other processor cores of the SoC.

High-performance interconnects provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals. The device also offers a comprehensive clock-management scheme.

One on-chip analog to digital converter (ADC0) can couple with the display subsystem to provide an integrated touch-screen solution. The other ADC (ADC1) can combine with the pulse width module to create a closed-loop motor control solution.

The real-time clock (RTC) provides a clock reference on a separate power domain. The clock reference enables a battery-backed clock reference.

The camera interface offers configuration for a single- or dual-camera parallel port.

Cryptographic acceleration is available in every AM437x device. Secure boot can also be made available for anticloning and illegal software update protection.

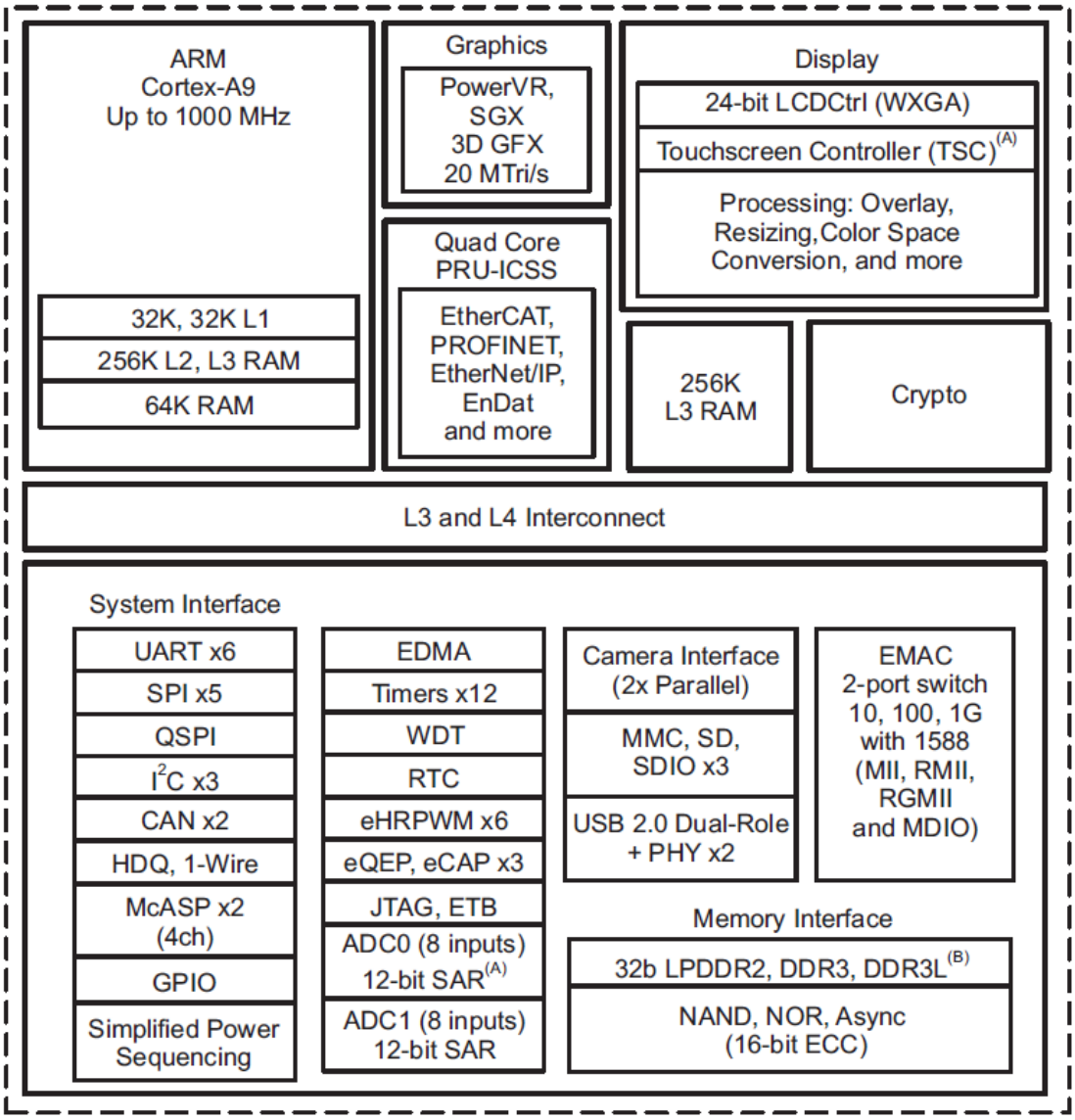


Figure 2-1. Functional Block Diagram

2.1.2 Memory

- **DDR3**

AM437x provides a memory controller for the expansion of external dynamic storage space. SBC-EC8800 extends two DDR3L SDRAM devices from Micron (The part number is MT41K256M16TW-107), and can provide 1GB external RAM access space.

Schematic as shown below:

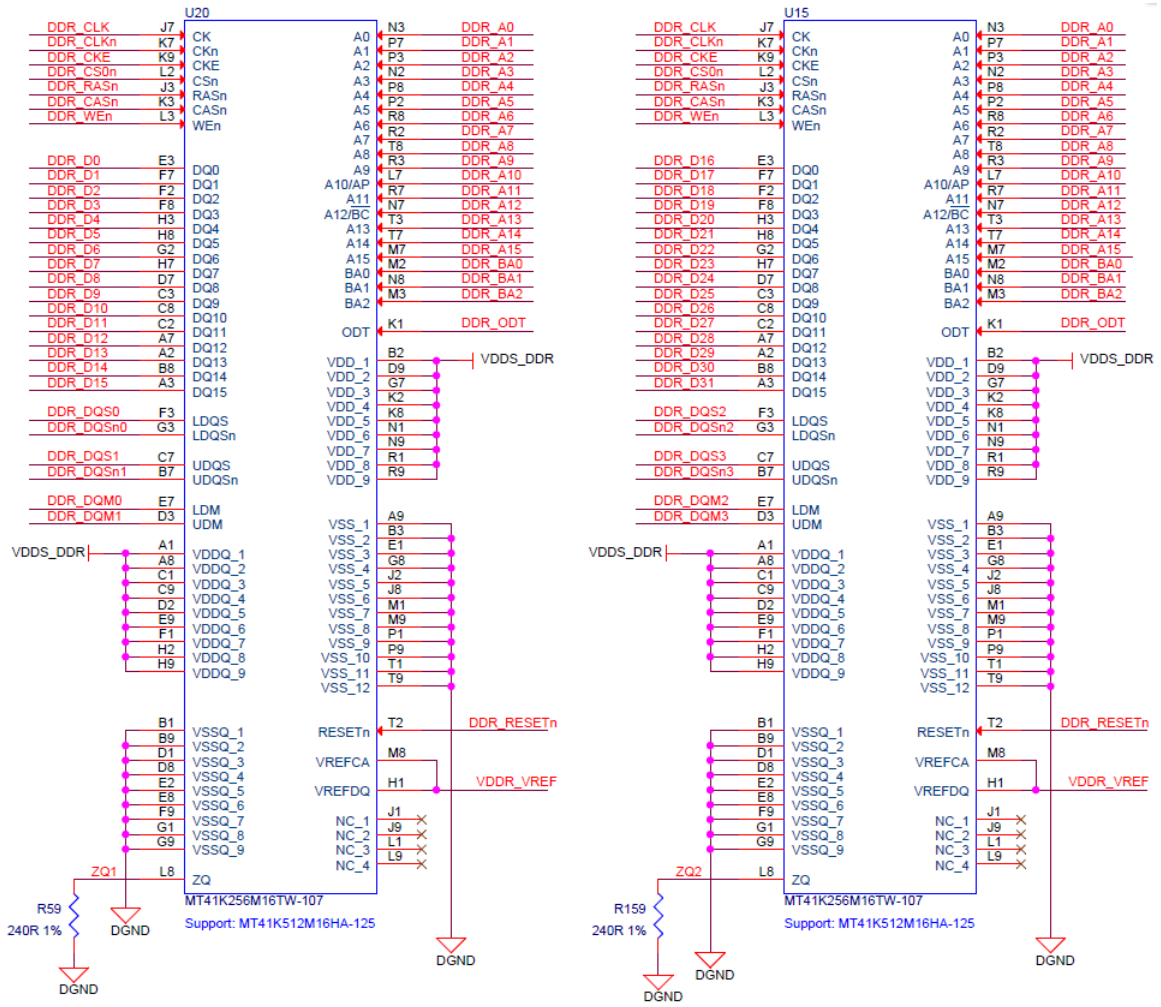


Figure 2-2. DDR3

- **QSPI Flash**

SBC-EC8800 board contains a 32MB QSPI Flash, model for N25Q256A13EF840. The QSPI can be used for booting, and the remaining storage space can also be used to store file.

If QSPI Flash has been burned to a boot loader, SBC-EC8800 will run the software system from QSPI Flash, detailed in the introduction, referring to the software manual.

Schematic as shown below:

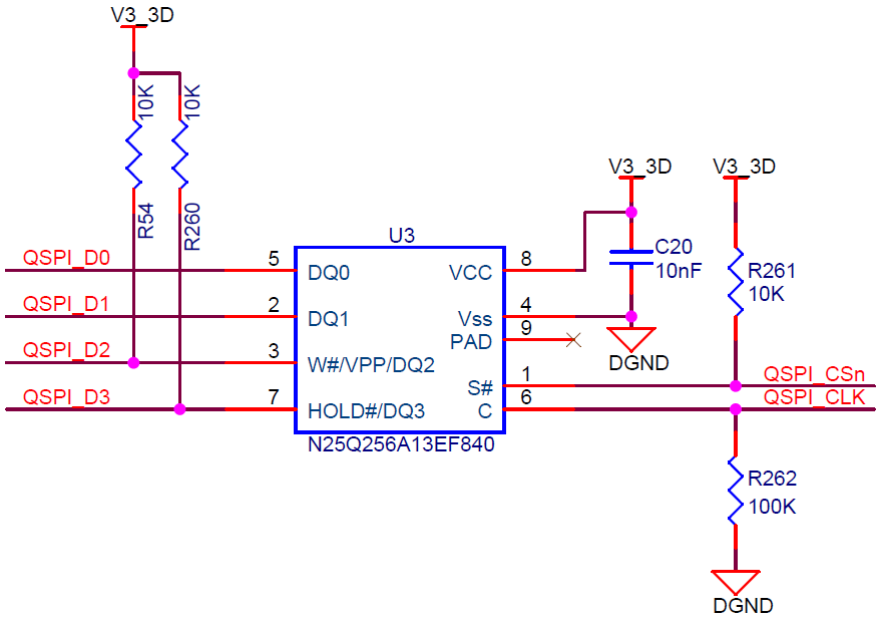


Figure 2-3. QSPI Flash

- **eMMC Flash**

AM437x provides three MMC interfaces, that can support the memory card and eMMC memory, SBC-EC8800 board contains a 4GB eMMC Flash, using MMC1 bus.

Schematic as shown below:

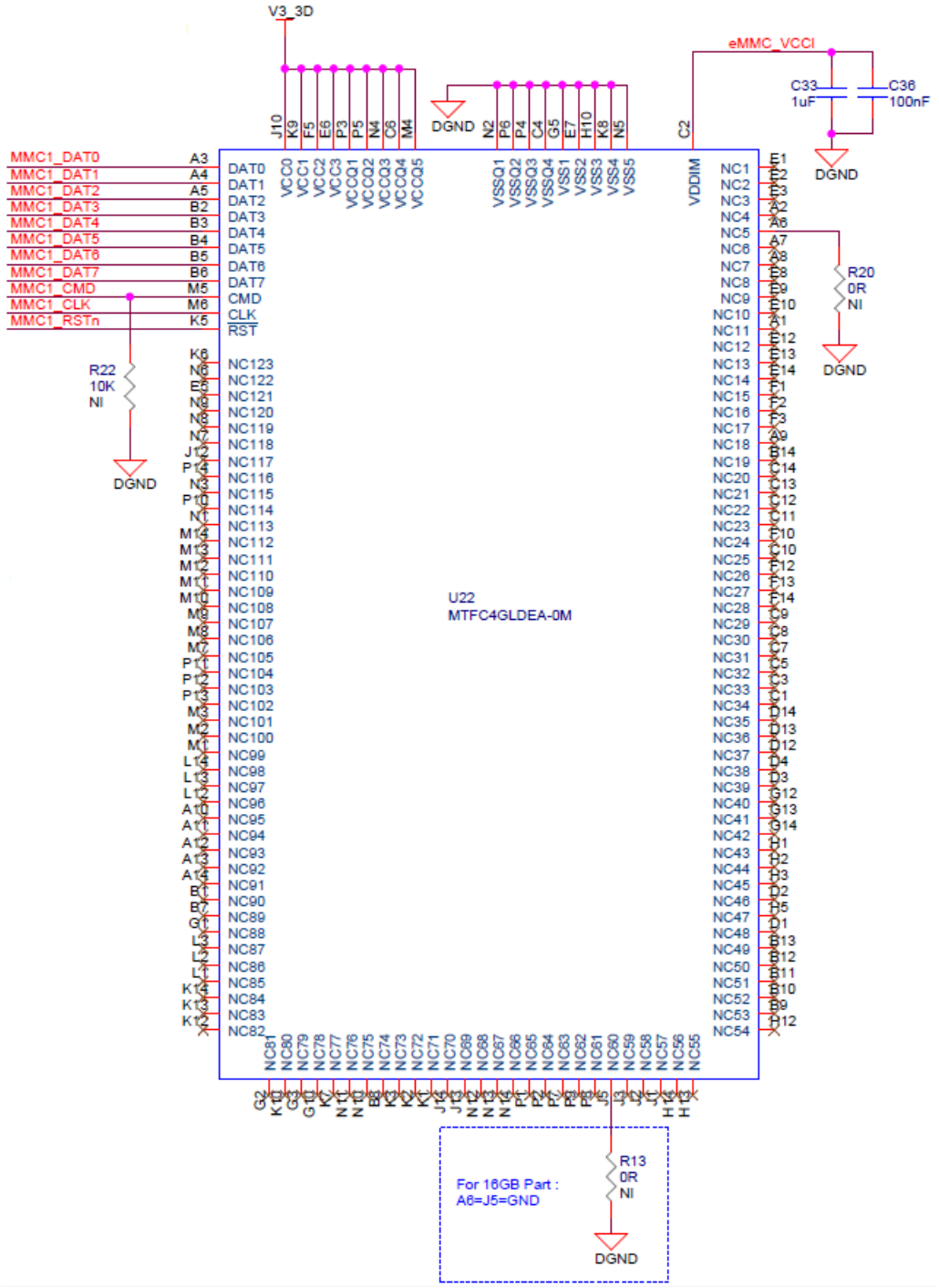


Figure 2-4. eMMC

- **EEPROM**

SBC-EC8800 board contains a 32KB EEPROM, by P/N CAT24C256W. As a non-volatile memory, the memory can be used to store some important information, such as the board configuration information, etc.

Schematic as shown below:

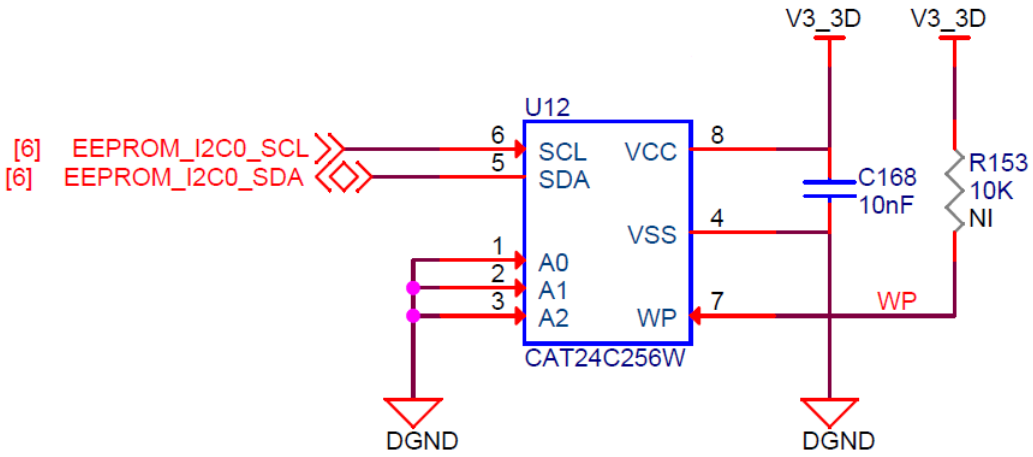


Figure 2-5. EEPROM

2.1.3 PMIC

SBC-EC8800 board contains the power management chip TPS65218, the chip is a high-performance PMIC launched by TI for AM437x and AM335x specifically, including the multi-channel power output, used to support the various power for AM437x.

SBC-EC8800 is powered through the DC power supply socket J7 with recommended input voltage 5V, ranged from 4.5V to 5.5V. When the input voltage exceeds 5.5V, the power input protection circuit will disconnect the input power supply and PMIC chip connection automatically, and the red LED D7 which is the over voltage indicator will turn on. When the input power supply voltage is normal, the D7 will turn off, and the green LED D10 will turn on, it means that PMIC is working normally.

The RTC backup power supply is used through the J12, the recommended use of 3V coin-cell battery, allowing the voltage range of 2.2V to 3.3V. If not use, this interface cannot be connected, and be left floating.

Schematic as shown below:

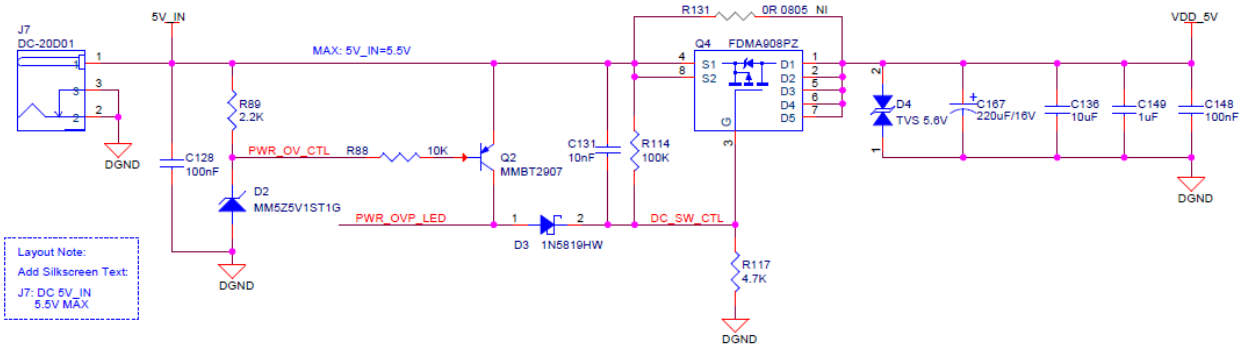


Figure 2-6. Input Power Overvoltage Protection Circuit

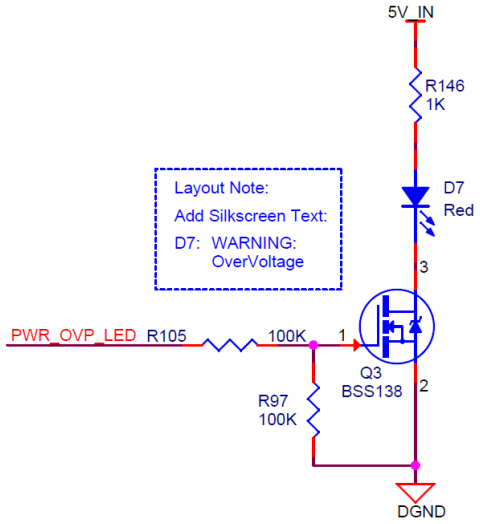


Figure 2-7. Input Power Overvoltage Indicator LED

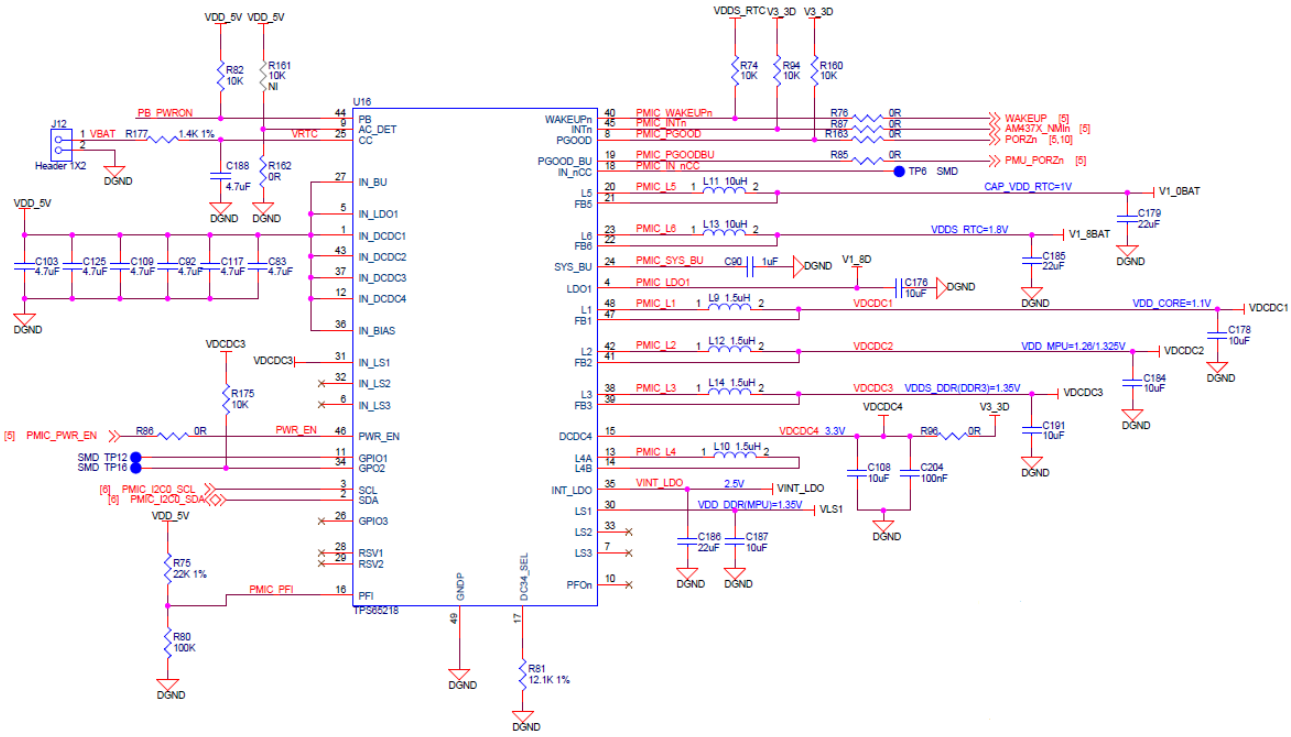


Figure 2-8. PMIC Circuit

2.2 External interface

To make users understand the board's hardware circuit better, this section will describe the structure, working principle, interface definition, etc.

2.2.1 LED

There are three green LED on the SBC-EC8800. D10 is 3.3V power indicator LED, and be on when the system is being powered on; D8 and D9 are programmable LED, user can control the LED using GPIO.

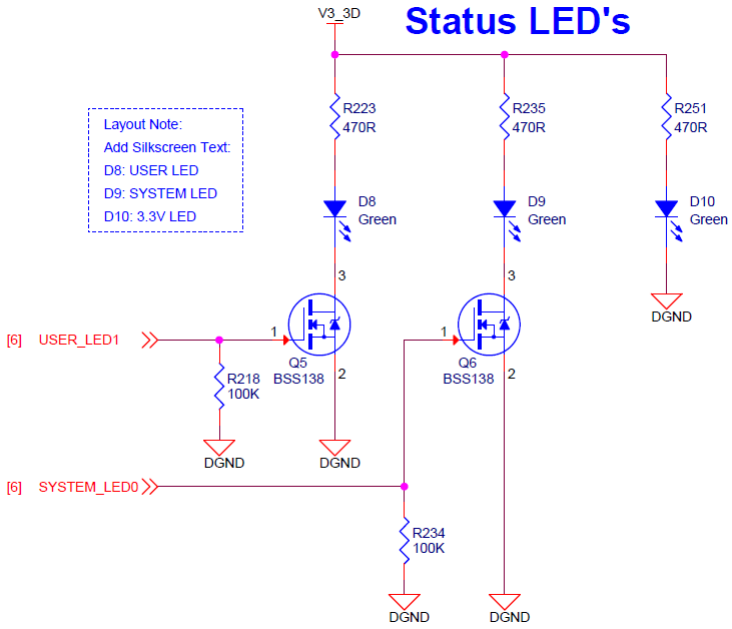


Figure 2-9. LED

2.2.2 Button and DIP Switch

SBC-EC8800 provides three buttons and one DIP switch, which SW1 for the Power ON/OFF button, SW2 for the Reset button, SW4 for the Boot selection button, SW3 for the Boot select DIP switch, respectively, as follows:

- **Power ON/OFF Button**

SW1 is connected to the Pin44 of U16 which is the PMIC, can be used to power-up the board. If you want to know more information about the Pin, please refer to the Datasheet of TPS65218.

The button is DNP (Do Not Place) by default, so the power output of the SBC-EC8800 is not controlled by this button, that is, when the power supply to the board, PMIC will power on automatically.

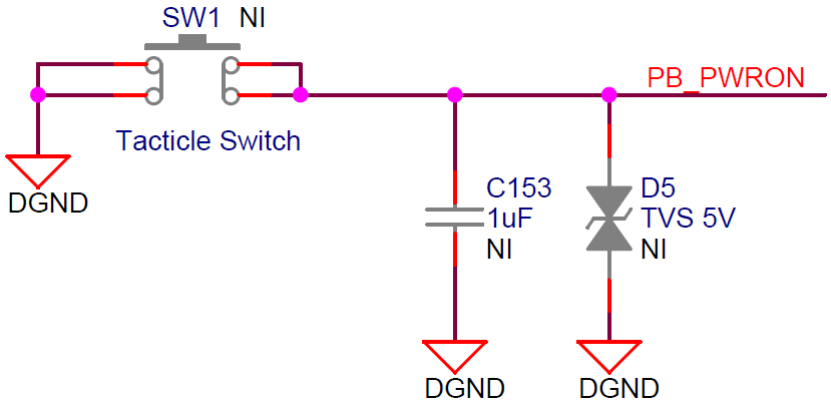


Figure 2-10. Power ON/OFF Button

- **Reset Button**

SW2 for the hardware reset button, press this button, the system will reset, than reboot the board.

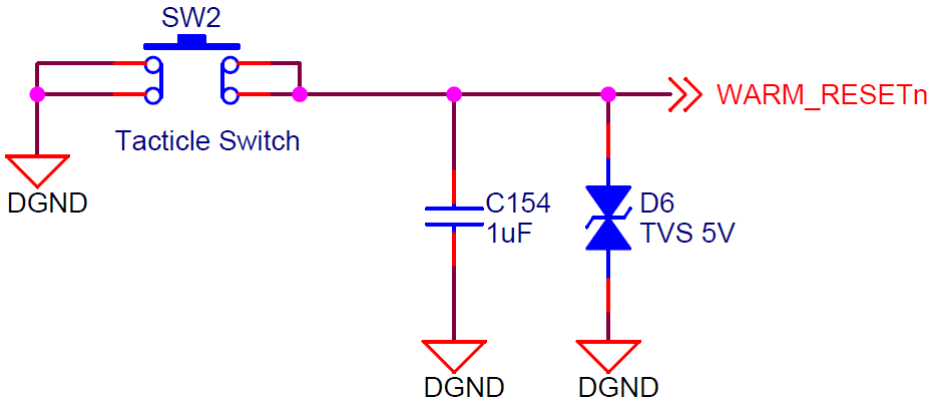
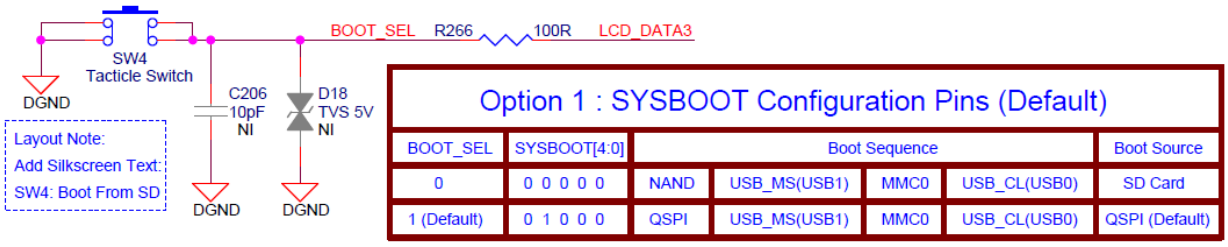


Figure 2-11. Reset Button

- **Boot Configuration Button**

SW4 is the Boot configuration button, and can be configured to change the boot order. Without holding the button, the board will try to boot from the QSPI Flash. If it is empty, then it will try booting from the MicroSD slot. If you hold the boot switch down during the removal and reapplication of power to the board, and you have a MicroSD card inserted with a bootable image, the board will boot from the MicroSD card.



Option 1 : SYSBOOT Configuration Pins (Default)

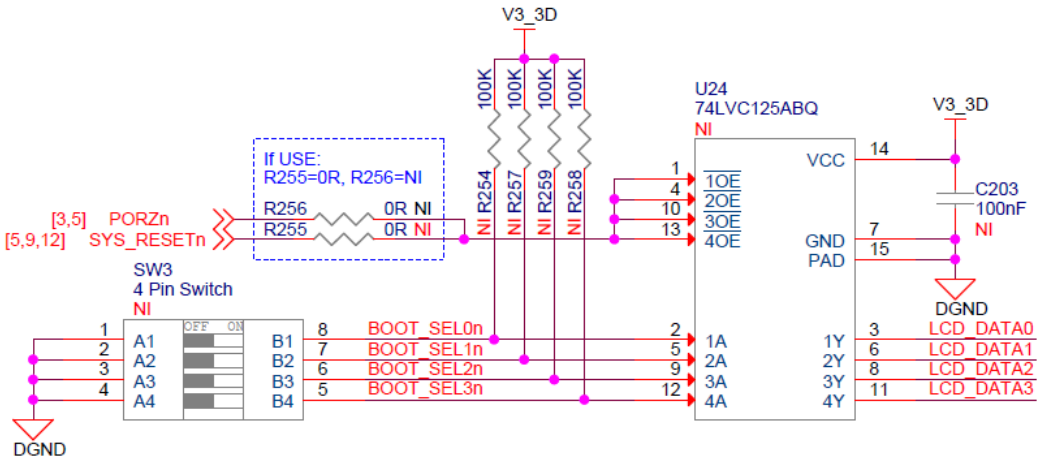
BOOT_SEL	SYSBOOT[4:0]	Boot Sequence				Boot Source
0	0 0 0 0 0	NAND	USB_MS(USB1)	MMC0	USB_CL(USB0)	SD Card
1 (Default)	0 1 0 0 0	QSPI	USB_MS(USB1)	MMC0	USB_CL(USB0)	QSPI (Default)

Figure 2-12. Boot Configuration Button

- **Boot Configuration DIP Switch**

SW3 is a four-channel DIP switch, the DIP switch and the surrounding components constitute a group of Boot configuration circuit, this part of the circuit has the same functions with SW4, and can configure the board booting from the QSPI flash, or MicroSD card.

This part of the circuit is a backup circuit, so these components are not placed standard on the board. To use this, these components in **Figure 2-13** will need to be soldered onto the board.



Option 2 : SYSBOOT Configuration Pins

NA	BOOT_SEL3	BOOT_SEL2	BOOT_SEL1	BOOT_SEL0	SYSBOOT[4:0]	Boot Source
SYSBOOT4	SYSBOOT3	SYSBOOT2	SYSBOOT1	SYSBOOT0		
0	1	0	1	0	0 1 0 1 0	QSPI
0	1	1	0	0	0 1 1 0 0	SD Card

Figure 2-13. Boot Configuration DIP Switch

2.2.3 Ethernet

SBC-EC8800 provides a 10/100/1000 Mbps three speed Ethernet interface, RGMII1 as the use of bus, PHY transceiver using MICREL company's KSZ9031, interface through the RJ45 terminal, the part reference number is J8, schematic as shown below:

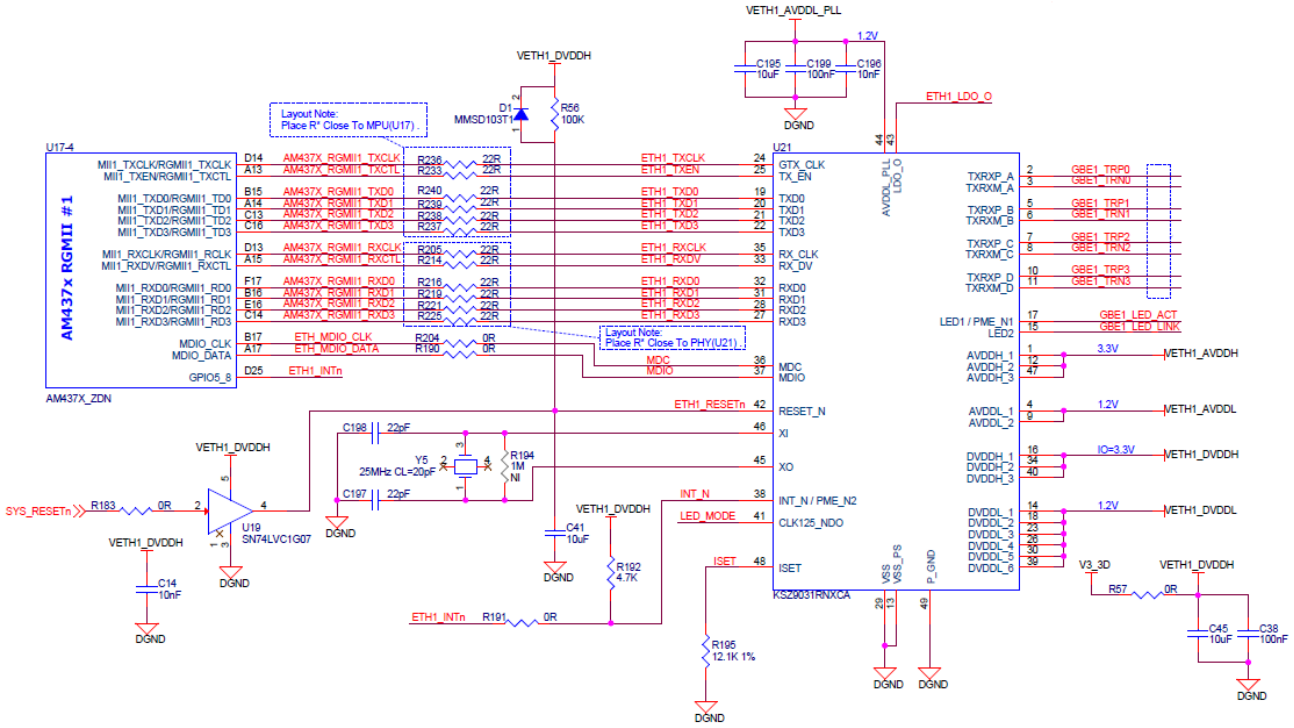


Figure 2-14. Ethernet Circuit

2.2.4 USB

SBC-EC8800 provides two USB 2.0 interfaces. The power switch IC is SP2526A-1EN-L which is a dual USB high-side power switch. Each USB can supply 5V 500mA minimum, and the fault currents are limited to 1.0A typical and the flag output pin for each switch is available to indicate fault conditions to the CPU controller.

The schematic as shown:

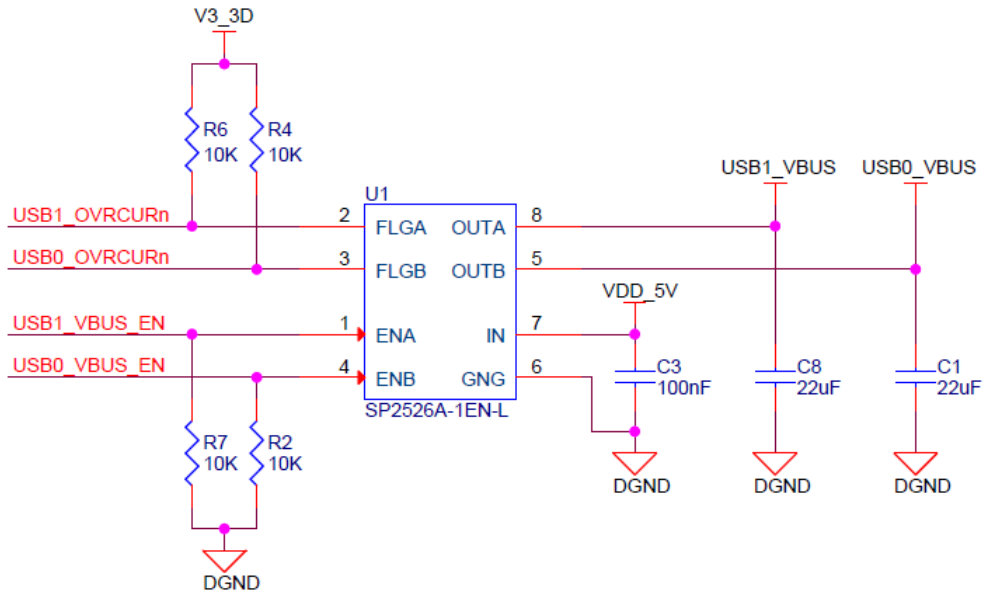


Figure 2-15. USB Power

USB0 is the OTG USB interface, which uses the standard Micro USB AB connector.

The schematic as shown:

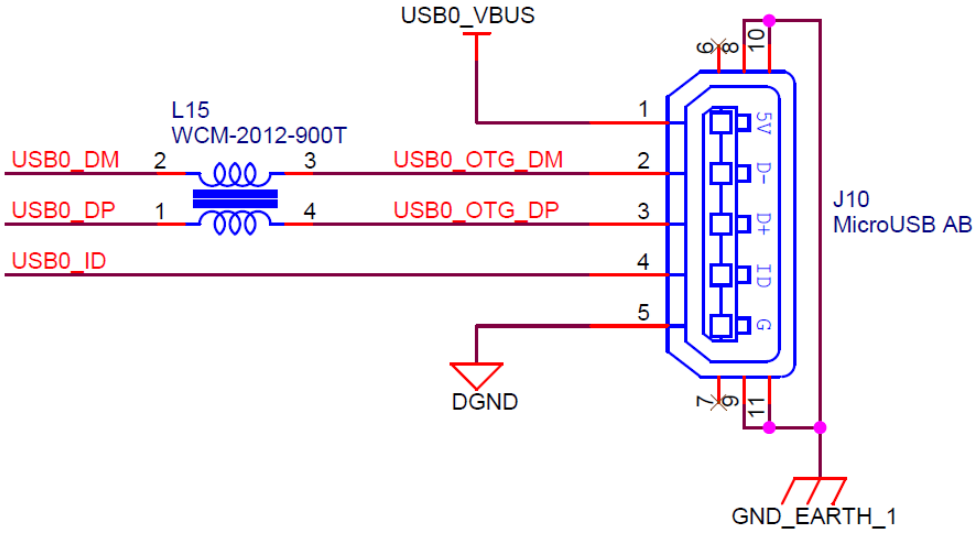


Figure 2-16. USB OTG

USB1 is the Host USB interface, which uses a single USB Type A female connector.

The schematic as shown:

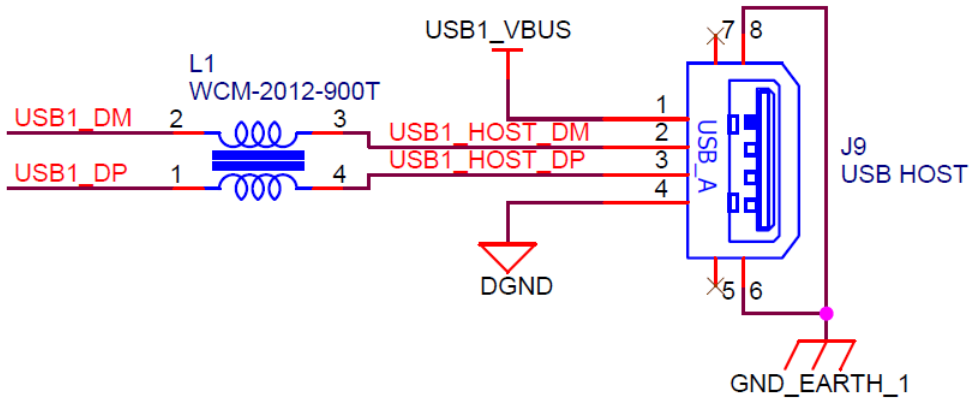


Figure 2-17. USB Host

2.2.5 UART

There are four UARTs on SBC-EC8800 board, UART0 of these is the debug UART, to be input and output interface of the information from system as default. UART1 is connected to the expansion interface J11, UART3 with flow control is converted to RS485, and UART5 with flow control is connected to Bluetooth module and is multiplexed to J11.

Debug UART0 is isolated by the buffer chip SN74LVC2G241, and is connected to J13 which is 2.54MM connector. And the level of signal is 3.3V CMOS.

The schematic as shown below:

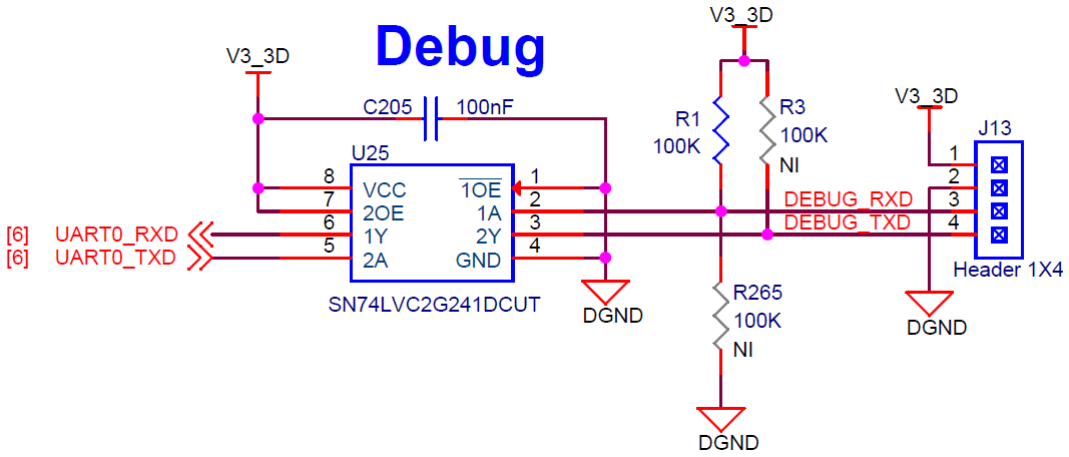


Figure 2-18. Debug UART

2.2.6 WLAN+Bluetooth

SBC-EC8800 provides one WLAN+Bluetooth interface, the function block diagram as the **Figure 2-19**. Please refer to the schematic and datasheet of WG7831-D0 for more information.

NOTE:

This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

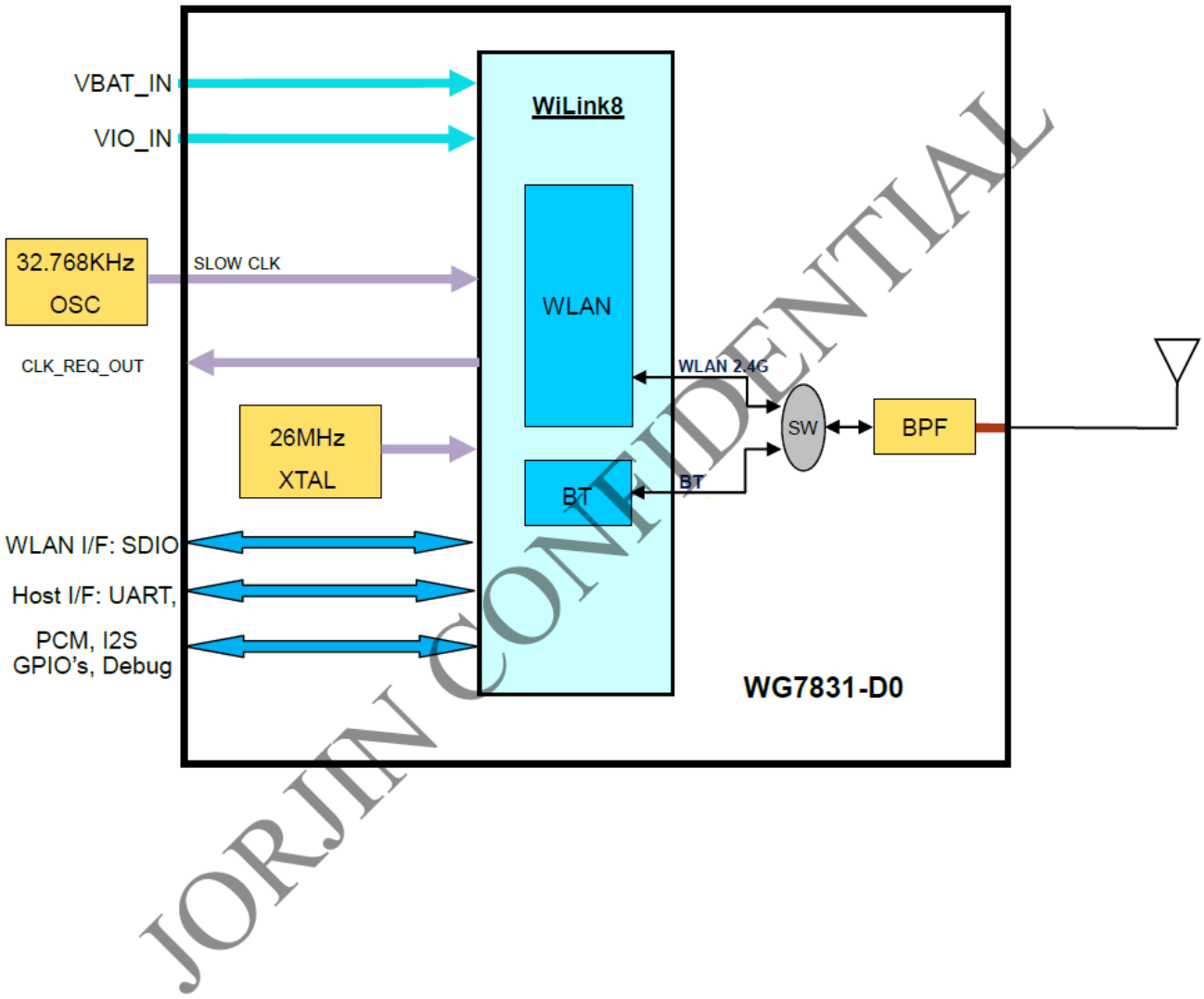


Figure 2-19. WLAN+Bluetooth Function Block Diagram

WLAN and Bluetooth Features as follows:

◆ **WLAN Features**

- Integrated 2.4 GHz Power Amplifier (PA) for WLAN solution
- WLAN MAC Baseband Processor and RF transceiver - IEEE802.11b/g/n compliant
- WLAN 11n 40MHz (SISO) and 11n 20MHz (SISO)
- Baseband Processor
  - IEEE Std 802.11b/g/n data rates and IEEE Std 802.11n data rates up to 40 MHz SISO
- Fully calibrated system. No production calibration required
- Medium Access Controller (MAC)
  - Embedded ARM™ Central Processing Unit (CPU)
  - Hardware-Based Encryption/Decryption using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys

- Supports requirements for Wireless Fidelity (Wi-Fi) Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [includes hardware-accelerated Advanced Encryption Standard (AES)]
- Designed to work with IEEE Std 802.1x

- IEEE Std 802.11d, e, h, i, k, r PICS compliant
- New advanced co-existence scheme with BT
- 802.11V supports for high-precision timing and location approximation
- Supports 4 bit SDIO host interface, including high speed (HS) and V3 modes

◆ **Bluetooth Features**

- Supports Bluetooth 4.0 BLE
- Includes built -in coexistence and prioritization handling for BT, BLE, ANT, and WLAN
- Dedicated Audio processor supporting on chip SBC encoding + A2DP:
  - Assisted A2DP (A3DP) support - SBC encoding implemented internally
  - Assisted WB-Speech (AWBS) support - modified SBC codec implemented internally

2.2.7 RS485

SBC-EC8800 provides one RS485 interface, using the ADM3485 from Analog Devices as the transceiver IC, networking applications as follows:

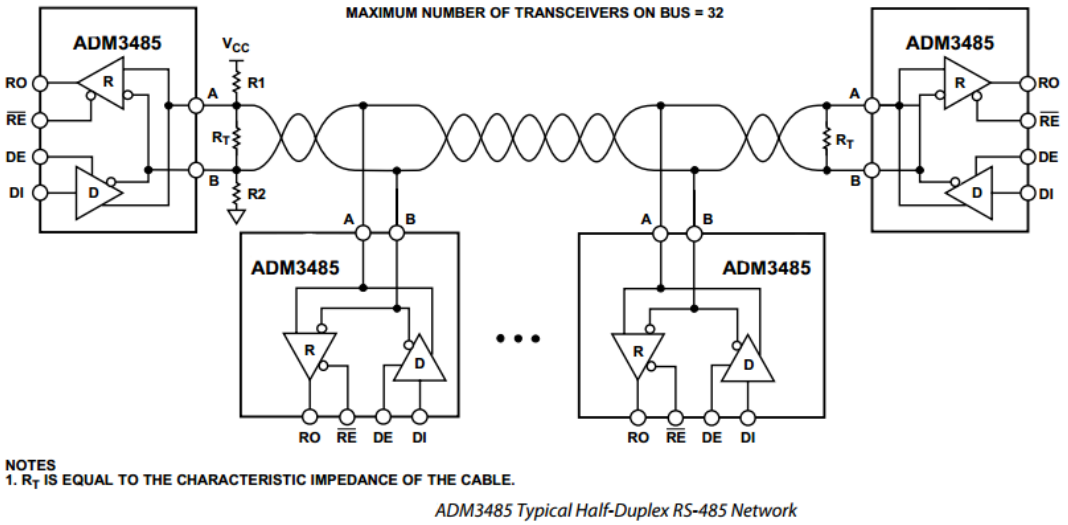


Figure 2-20. RS485 Networking

The board uses UART3 to achieve RS485 communication with the ESD protection. The RS485 bus is connected to the expansion interface J5.

The schematic as follows:

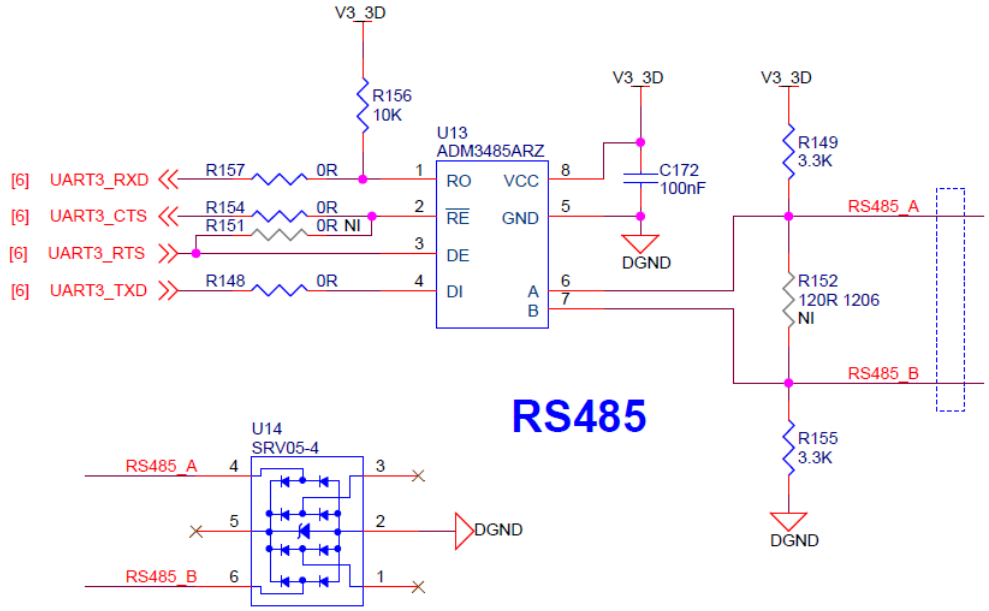


Figure 2-21. RS485 Bus

2.2.8 CAN

SBC-EC8800 provides two CAN buses with ESD protection, The CAN controller is integrated in the CPU, and the transceiver uses MC33901 from NXP. Two CAN buses are connected to the expansion interface J5.

The schematic as follows:

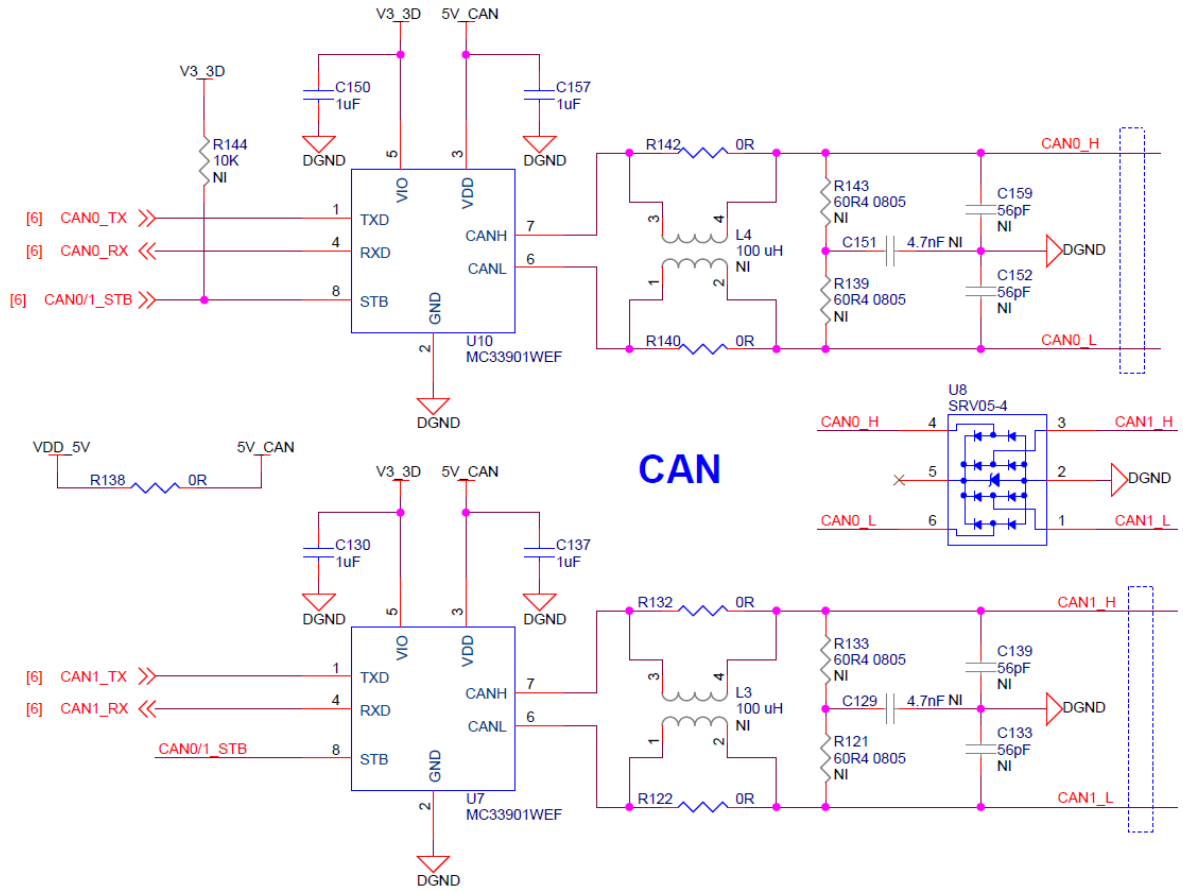


Figure 2-22. CAN Bus

2.2.9 MicroSD

A MicroSD connector is located on the backside of the board, and the bus uses MMC0, 4bit data width.

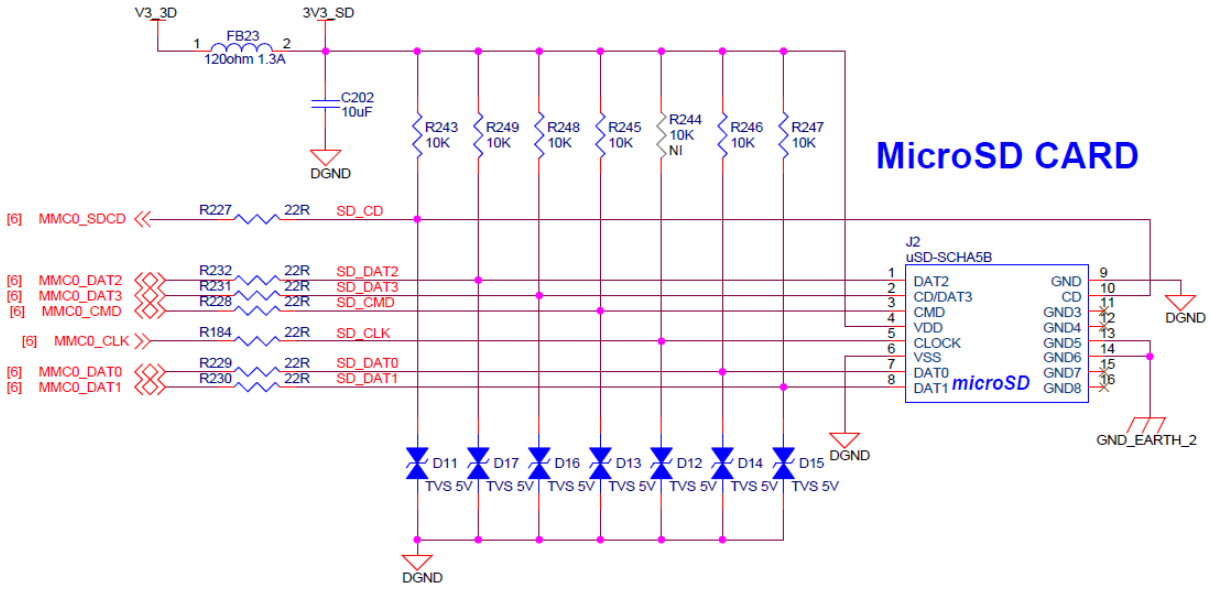


Figure 2-23. MicroSD

2.2.10 LCD

SBC-EC8800 provides one 24Bit RGB LCD interface, the part location number is J1, interface definition and signal description as shown in **Figure 2-24** and **Table 2-1**:

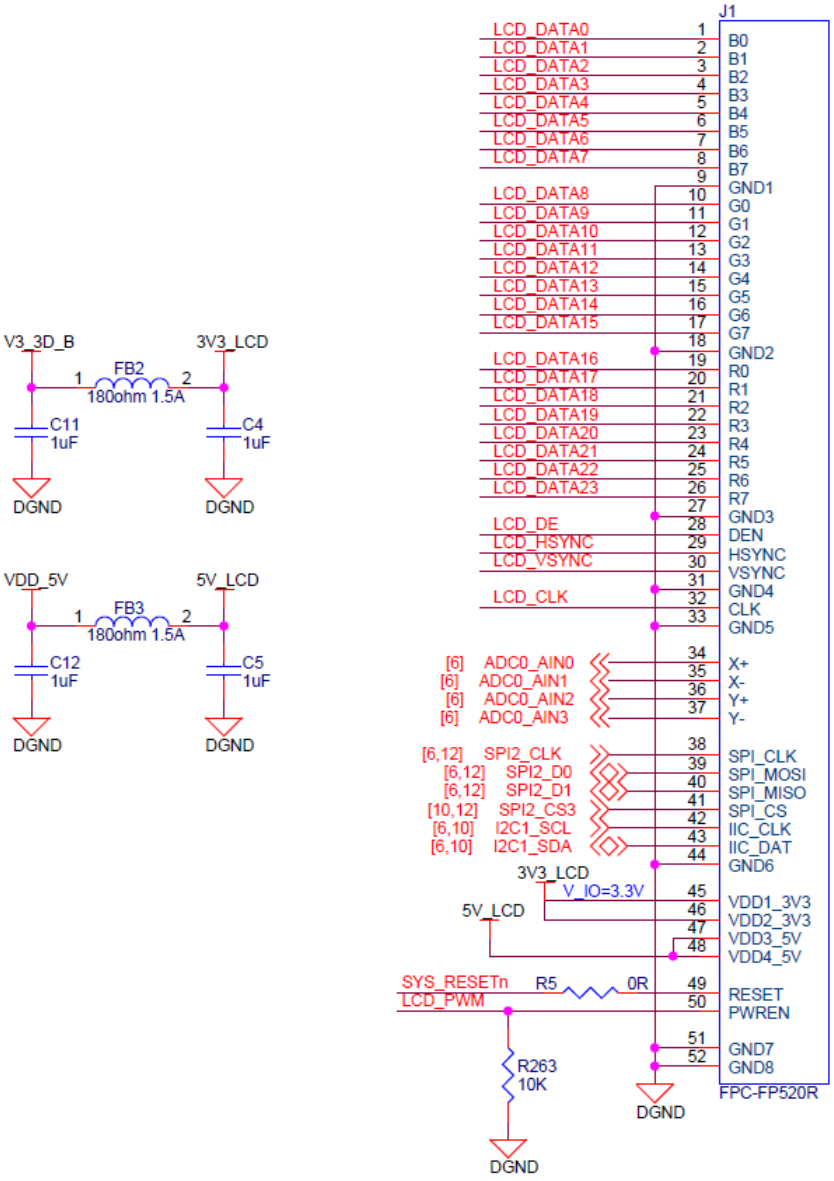


Figure 2-24. LCD Interface

Table 2-1. LCD Interface J1 Specification

Pin	Signal Name	Direction	Type / Tolerance	Description
1	LCD_DATA0	Output	CMOS 3.3V	8 bit Blue color data
2	LCD_DATA1	Output	CMOS 3.3V	
3	LCD_DATA2	Output	CMOS 3.3V	
4	LCD_DATA3	Output	CMOS 3.3V	

5	LCD_DATA4	Output	CMOS 3.3V	
6	LCD_DATA5	Output	CMOS 3.3V	
7	LCD_DATA6	Output	CMOS 3.3V	
8	LCD_DATA7	Output	CMOS 3.3V	
9	GND		Ground	Signal and power return, and GND reference
10	LCD_DATA8	Output	CMOS 3.3V	8 bit Green color data
11	LCD_DATA9	Output	CMOS 3.3V	
12	LCD_DATA10	Output	CMOS 3.3V	
13	LCD_DATA11	Output	CMOS 3.3V	
14	LCD_DATA12	Output	CMOS 3.3V	
15	LCD_DATA13	Output	CMOS 3.3V	
16	LCD_DATA14	Output	CMOS 3.3V	
17	LCD_DATA15	Output	CMOS 3.3V	
18	GND		Ground	Signal and power return, and GND reference
19	LCD_DATA16	Output	CMOS 3.3V	8 bit RED color data
20	LCD_DATA17	Output	CMOS 3.3V	
21	LCD_DATA18	Output	CMOS 3.3V	
22	LCD_DATA19	Output	CMOS 3.3V	
23	LCD_DATA20	Output	CMOS 3.3V	
24	LCD_DATA21	Output	CMOS 3.3V	
25	LCD_DATA22	Output	CMOS 3.3V	
26	LCD_DATA23	Output	CMOS 3.3V	
27	GND		Ground	Signal and power return, and GND reference
28	LCD_DE	Output	CMOS 3.3V	Display Enable
29	LCD_HSYNC	Output	CMOS 3.3V	Horizontal Sync
30	LCD_VSYNC	Output	CMOS 3.3V	Vertical Synch
31	GND		Ground	Signal and power return, and GND reference
32	LCD_CLK	Output	CMOS 3.3V	Pixel clock
33	GND		Ground	Signal and power return, and GND reference
34	ADC0_AIN0	Input	Analog 1.8V	Analog Signal input
35	ADC0_AIN1	Input	Analog 1.8V	Analog Signal input
36	ADC0_AIN2	Input	Analog 1.8V	Analog Signal input
37	ADC0_AIN3	Input	Analog 1.8V	Analog Signal input
38	SPI2_CLK	Output	CMOS 3.3V	SPI Master Clock output
39	SPI2_D0	Output	CMOS 3.3V	SPI Master Data output (output from CPU, input to SPI device)
40	SPI2_D1	Input	CMOS 3.3V	SPI Master Data input (input to CPU, output from SPI

				device)
41	SPI2_CS3	Output	CMOS 3.3V	SPI Master Chip Select output
42	I2C1_SCL	Bi-Dir OD	CMOS 3.3V	I2C data signal
43	I2C1_SDA	Bi-Dir OD	CMOS 3.3V	I2C clock signal
44	GND		Ground	Signal and power return, and GND reference
45	3V3_LCD	Output	Power 3.3V	Power 3.3V output
46	3V3_LCD	Output	Power 3.3V	Power 3.3V output
47	5V_LCD	Output	Power 5V	Power 5V output
48	5V_LCD	Output	Power 5V	Power 5V output
49	SYS_RESETn	Output	CMOS 3.3V	General purpose reset output
50	LCD_PWM	Output	CMOS 3.3V	Display backlight PWM control
51	GND		Ground	Board Lock, Connect to GND
52	GND		Ground	Board Lock, Connect to GND

2.2.11 Camera

SBC-EC8800 provides one 12Bit Camera interface, the part location number is J3, interface definition and signal description as shown in **Figure 2-25** and **Table 2-2**:

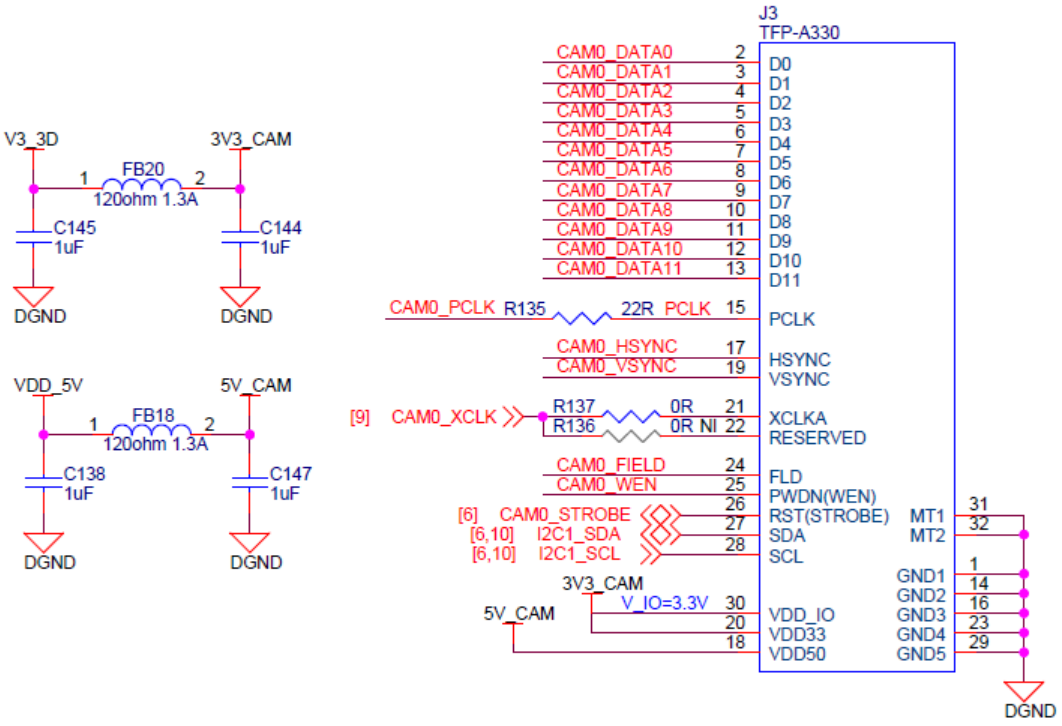


Figure 2-25. Camera Interface

Table 2-2. Camera Interface J3 Specification

Pin	Signal Name	Direction	Type / Tolerance	Description
1	GND		Ground	Signal and power return, and GND reference
2	CAM0_DATA0	Input	CMOS 3.3V	Parallel camera input data
3	CAM0_DATA1	Input	CMOS 3.3V	
4	CAM0_DATA2	Input	CMOS 3.3V	
5	CAM0_DATA3	Input	CMOS 3.3V	
6	CAM0_DATA4	Input	CMOS 3.3V	
7	CAM0_DATA5	Input	CMOS 3.3V	
8	CAM0_DATA6	Input	CMOS 3.3V	
9	CAM0_DATA7	Input	CMOS 3.3V	
10	CAM0_DATA8	Input	CMOS 3.3V	
11	CAM0_DATA9	Input	CMOS 3.3V	
12	CAM0_DATA10	Input	CMOS 3.3V	
13	CAM0_DATA11	Input	CMOS 3.3V	
14	GND		Ground	Signal and power return, and GND reference
15	CAM0_PCLK	Input	CMOS 3.3V	CCD Data Pixel Clock
16	GND		Ground	Signal and power return, and GND reference
17	CAM0_HSYNC	Input	CMOS 3.3V	CCD Data Horizontal Detect
18	5V_CAM	Output	Power 5V	Power 5V output
19	CAM0_VSYNC	Input	CMOS 3.3V	CCD Data Vertical Detect
20	3V3_CAM	Output	Power 3.3V	Power 3.3V output
21	CAM0_XCLK	Output	CMOS 3.3V	Parallel camera Master Clock output
22	RESERVED	Output	CMOS 3.3V	No signal
23	GND		Ground	Signal and power return, and GND reference
24	CAM0_FIELD	Input	CMOS 3.3V	CCD Data Field Indicator
25	CAM0_WEN	Input	CMOS 3.3V	CCD Data Write Enable
26	CAM0_STROBE	Output	CMOS 3.3V	GPIO
27	I2C1_SDA	Bi-Dir OD	CMOS 3.3V	I2C data signal
28	I2C1_SCL	Bi-Dir OD	CMOS 3.3V	I2C clock signal
29	GND		Ground	Signal and power return, and GND reference
30	3V3_CAM	Output	Power 3.3V	Power 3.3V output
31	GND		Ground	Board Lock, Connect to GND
32	GND		Ground	Board Lock, Connect to GND

2.2.12 Expansion Interface

There are some unused IOs from AM437x in SBC-EC8800, and are connected to the J5 and J11 which are 2*20Pin expansion headers. These IOs can be used as GPIO, and also can be configured as bus, such as SPI, IIC, etc.

There are one RS485 and two CAN bus in J5, and can be used as serial interfaces.

Interface definition and signal description as shown in **Figure 2-26**, **Table 2-3** and **Table 2-4**:

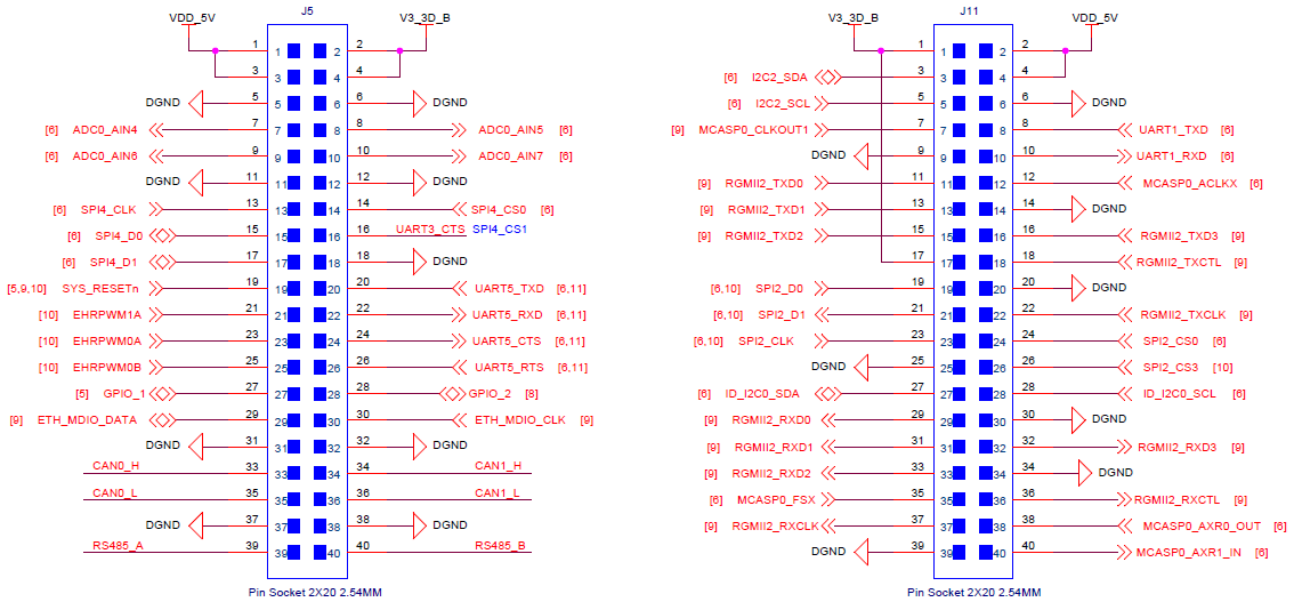


Figure 2-26. Expansion Connectors

Table 2-3. Expansion Connector J5 Specification

Pin	Signal Name	Direction	Type / Tolerance	Description
1	VDD_5V	Output	Power 5V	Power 5V output
2	V3_3D_B	Output	Power 3.3V	Power 3.3V output
3	VDD_5V	Output	Power 5V	Power 5V output
4	V3_3D_B	Output	Power 3.3V	Power 3.3V output
5	GND		Ground	Signal and power return, and GND reference
6	GND		Ground	Signal and power return, and GND reference
7	ADC0_AIN4	Input	Analog 1.8V	Analog Signal input
8	ADC0_AIN5	Input	Analog 1.8V	Analog Signal input
9	ADC0_AIN6	Input	Analog 1.8V	Analog Signal input
10	ADC0_AIN7	Input	Analog 1.8V	Analog Signal input
11	GND		Ground	Signal and power return, and GND reference
12	GND		Ground	Signal and power return, and GND reference
13	SPI4_CLK	Output	CMOS 3.3V	SPI Master Clock output

14	SPI4_CS0	Output	CMOS 3.3V	SPI Master Chip Select output
15	SPI4_D0	Output	CMOS 3.3V	SPI Master Data output (output from CPU, input to SPI device)
16	UART3_CTS	Input	CMOS 3.3V	SPI4_CS1
17	SPI4_D1	Input	CMOS 3.3V	SPI Master Data input (input to CPU, output from SPI device)
18	GND		Ground	Signal and power return, and GND reference
19	SYS_RESETn	Output	CMOS 3.3V	General purpose reset output
20	UART5_TXD	Output	CMOS 3.3V	UART Transmit Data
21	EHRPWM1A	Output	CMOS 3.3V	PWM(Pulse Width Modulation) Out
22	UART5_RXD	Input	CMOS 3.3V	UART Receive Data
23	EHRPWM0A	Output	CMOS 3.3V	PWM(Pulse Width Modulation) Out
24	UART5_CTS	Input	CMOS 3.3V	UART Clear to Send
25	EHRPWM0B	Output	CMOS 3.3V	PWM(Pulse Width Modulation) Out
26	UART5_RTS	Output	CMOS 3.3V	UART Request to Send
27	GPIO_1	Bi-Dir	CMOS 3.3V	General purpose input/output
28	GPIO_2	Bi-Dir	CMOS 3.3V	General purpose input/output
29	ETH_MDIO_DATA	Bi-Dir OD	CMOS 3.3V	MDIO Data
30	ETH_MDIO_CLK	Bi-Dir OD	CMOS 3.3V	MDIO CLK
31	GND		Ground	Signal and power return, and GND reference
32	GND		Ground	Signal and power return, and GND reference
33	CAN0_H	Bi-Dir	CAN	CAN Differential Signal +
34	CAN1_H	Bi-Dir	CAN	CAN Differential Signal +
35	CAN0_L	Bi-Dir	CAN	CAN Differential Signal -
36	CAN1_L	Bi-Dir	CAN	CAN Differential Signal -
37	GND		Ground	Signal and power return, and GND reference
38	GND		Ground	Signal and power return, and GND reference
39	RS485_A	Bi-Dir	RS485	RS485 Differential Signal +
40	RS485_B	Bi-Dir	RS485	RS485 Differential Signal -

Table 2-4. Expansion Connector J11 Specification

Pin	Signal Name	Direction	Type / Tolerance	Description
1	V3_3D_B	Output	Power 3.3V	Power 3.3V output
2	VDD_5V	Output	Power 5V	Power 5V output

3	I2C2_SDA	Bi-Dir OD	CMOS 3.3V	I2C data signal
4	VDD_5V	Output	Power 5V	Power 5V output
5	I2C2_SCL	Bi-Dir OD	CMOS 3.3V	I2C clock signal
6	GND		Ground	Signal and power return, and GND reference
7	MCASP0_CLKOUT1	Output	CMOS 3.3V	McASP0 Master clock output to Audio codec
8	UART1_TXD	Output	CMOS 3.3V	UART Transmit Data
9	GND		Ground	Signal and power return, and GND reference
10	UART1_RXD	Input	CMOS 3.3V	UART Receive Data
11	RGMII2_TXD0	Output	CMOS 3.3V	RGMII Transmit Data bit 0
12	MCASP0_ACLKX	Output	CMOS 3.3V	McASP0 Transmit Bit Clock
13	RGMII2_TXD1	Output	CMOS 3.3V	RGMII Transmit Data bit 1
14	GND		Ground	Signal and power return, and GND reference
15	RGMII2_TXD2	Output	CMOS 3.3V	RGMII Transmit Data bit 2
16	RGMII2_TXD3	Output	CMOS 3.3V	RGMII Transmit Data bit 3
17	V3_3D_B	Output	Power 3.3V	Power 3.3V output
18	RGMII2_TXCTL	Output	CMOS 3.3V	RGMII Transmit Control
19	SPI2_D0	Output	CMOS 3.3V	SPI Master Data output (output from CPU, input to SPI device)
20	GND		Ground	Signal and power return, and GND reference
21	SPI2_D1	Input	CMOS 3.3V	SPI Master Data input (input to CPU, output from SPI device)
22	RGMII2_TXCLK	Output	CMOS 3.3V	RGMII Transmit Clock
23	SPI2_CLK	Output	CMOS 3.3V	SPI Master Clock output
24	SPI2_CS0	Output	CMOS 3.3V	SPI Master Chip Select output
25	GND		Ground	Signal and power return, and GND reference
26	SPI2_CS3	Output	CMOS 3.3V	SPI Master Chip Select output
27	ID_I2C0_SDA	Bi-Dir OD	CMOS 3.3V	I2C data signal
28	ID_I2C0_SCL	Bi-Dir OD	CMOS 3.3V	I2C clock signal
29	RGMII2_RXD0	Input	CMOS 3.3V	RGMII Receive Data bit 0
30	GND		Ground	Signal and power return, and GND reference
31	RGMII2_RXD1	Input	CMOS 3.3V	RGMII Receive Data bit 1
32	RGMII2_RXD3	Input	CMOS 3.3V	RGMII Receive Data bit 3
33	RGMII2_RXD2	Input	CMOS 3.3V	RGMII Receive Data bit 2
34	GND		Ground	Signal and power return, and GND reference
35	MCASP0_FSX	Output	CMOS 3.3V	McASP0 Transmit Frame Sync

36	RGMII2_RXCTL	Input	CMOS 3.3V	RGMII Receive Control
37	RGMII2_RXCLK	Input	CMOS 3.3V	RGMII Receive Clock
38	MCASP0_AXR0 _OUT	Output	CMOS 3.3V	McASP0 Serial Data Out
39	GND		Ground	Signal and power return, and GND reference
40	MCASP0_AXR1 _IN	Input	CMOS 3.3V	McASP0 Serial Data In

Technical Support and Warranty

Technical Support

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- Helping customers properly compile and run the source code provided by Embest Technology;
- Providing technical support service if the embedded hardware products do not function properly under the circumstances that customers operate according to the instructions in the documents provided by Embest Technology;
- Helping customers troubleshoot the products.

The following conditions will not be covered by our technical support service. We will take appropriate measures accordingly:

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- Customers encounter issues caused by any unauthorized alter to the embedded operating system;
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- Products are damaged in appearance or function caused by power failure, external forces, water, animals or foreign materials;

- Products malfunction caused by disassembly or alter of components by customers or, products disassembled or repaired by persons or organizations unauthorized by Embest Technology, or altered in factory specifications, or configured or expanded with the components that are not provided or recognized by Embest Technology and the resulted damage in appearance or function;
- Product failures caused by the software or system installed by customers or inappropriate settings of software or computer viruses;;
- Products purchased from unauthorized sales;
- Warranty (including verbal and written) that is not made by Embest Technology and not included in the scope of our warranty should be fulfilled by the party who committed. Embest Technology has no any responsibility;

3） Within the period of warranty, the freight for sending products from customers to Embest Technology should be paid by customers; the freight from Embest to customers should be paid by us. The freight in any direction occurs after warranty period should be paid by customers;

4） Please contact technical support if there is any repair request.

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