SBC8118

INDEX

Design	Gary	Embest Technology Co., Ltd	
Review	Gary	TitleSBC8118	
Authorize	Gary	Size A3	Doc Name 01.CONVER PAGE / Ver. X2
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Schematic History

2012-07-09

1.Remove SATA 12 Power,and not support 3.5' hard disk.

2.Modify DM9161BIEP LED display function.

3.Modify buzzer logic function.

Design	Gary	**Embest Technology Co., Ltd**	
Review	Gary	TitleSBC8118	
Authorize	Gary	Size: A3	Doc Name: 02.Schematic History — Ver.: X2
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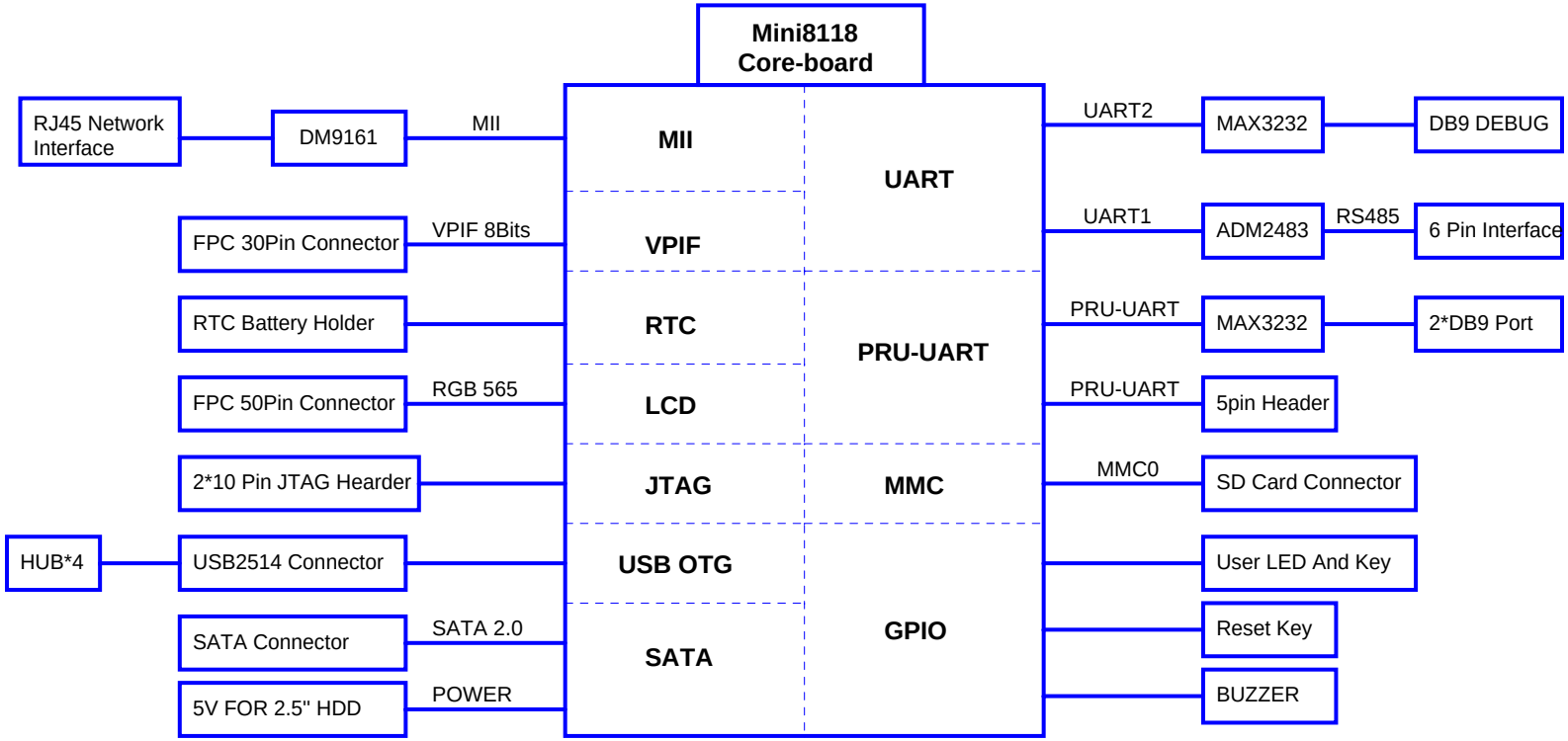

Design	Gary	**Embest Technology Co., Ltd**	
Review	Gary	TitleSBC8118	
Authorize	Gary	Size: A3 — Doc Name: 03.SYSTEM BLOCK	Ver.: X2
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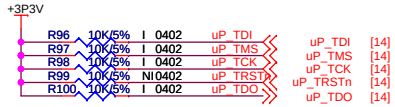
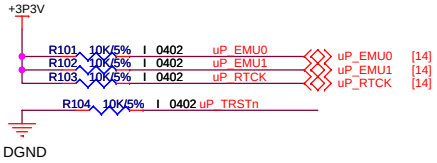
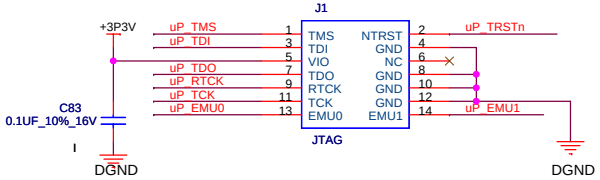
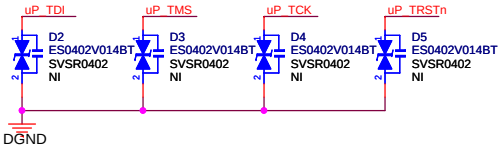
JTAG Interface

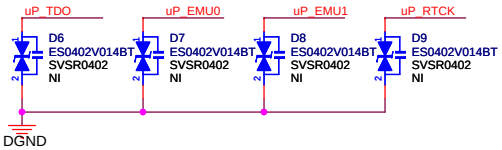




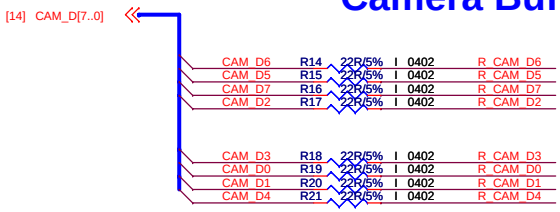


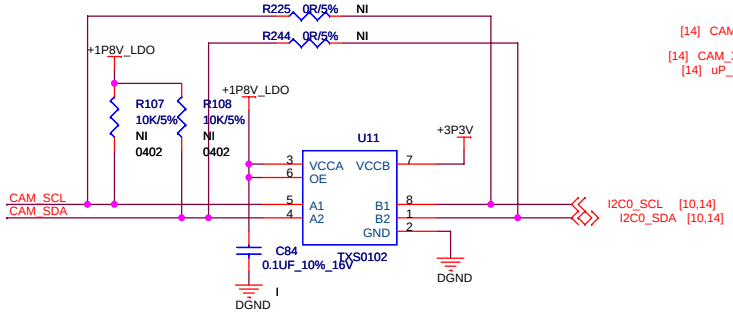
RTCLK,EMU0 and EMU1 is IO

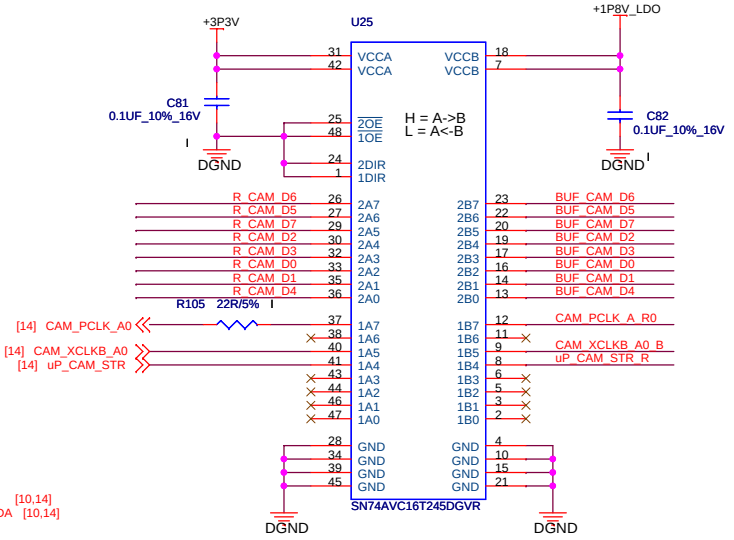




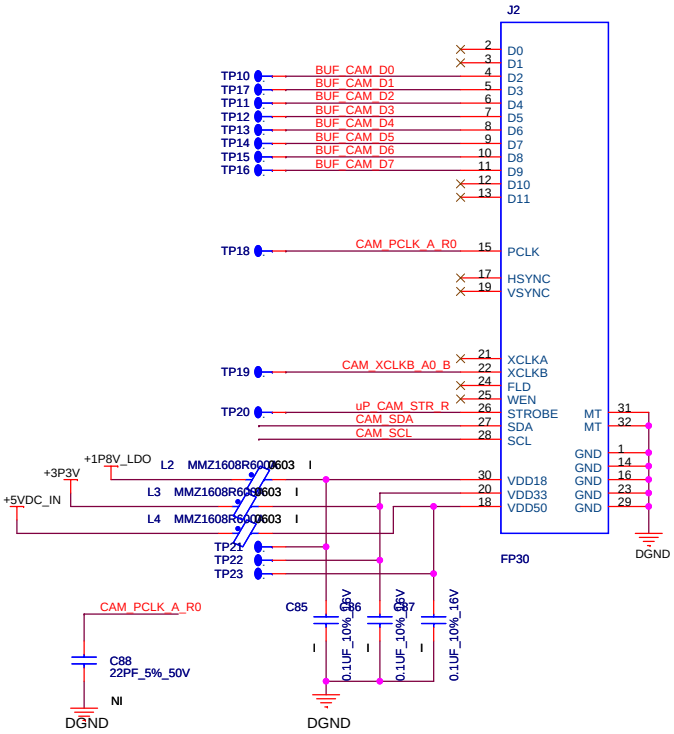
Camera Buffer

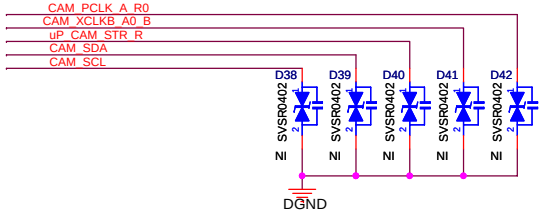


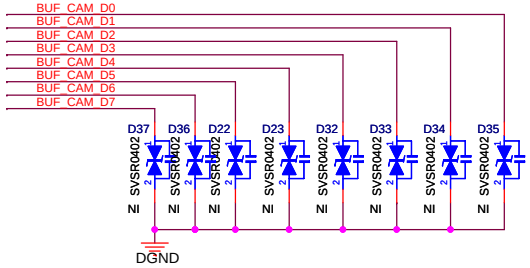




Camera Interface







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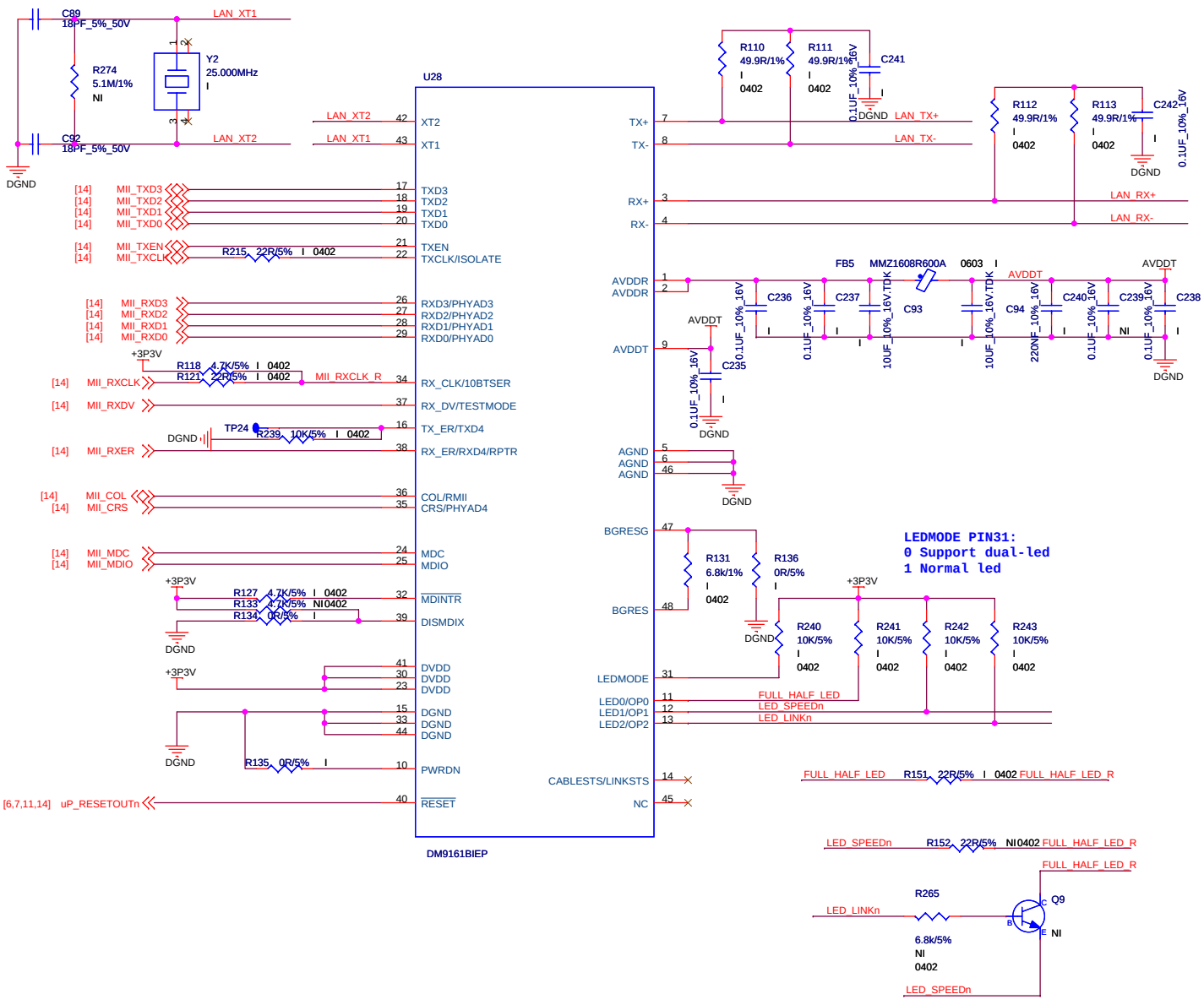
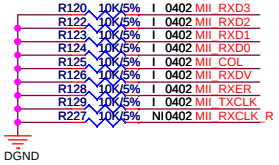
Ethernet Physical Layer



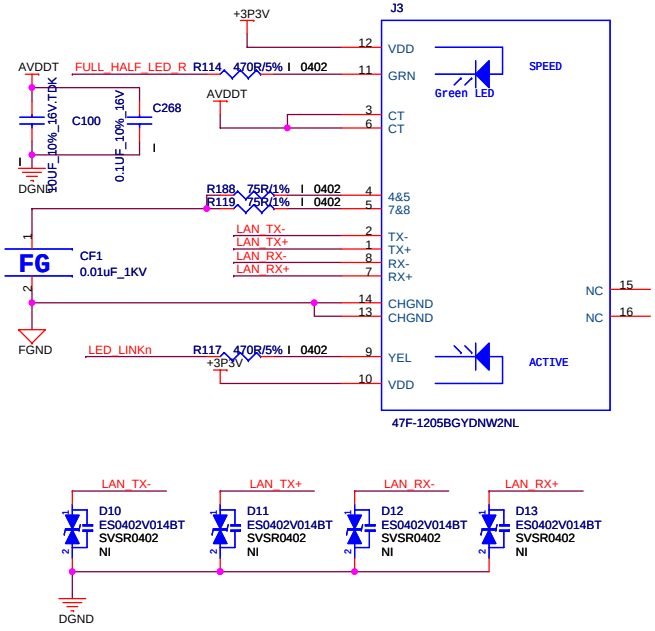
Strap Configuration



NOTE:DISMDIX=0,Enable
HP Auto-MIDX mode

Note:
100BASE-T RMII mode selected
(pin34 pull up ,default)

RJ45 Interface



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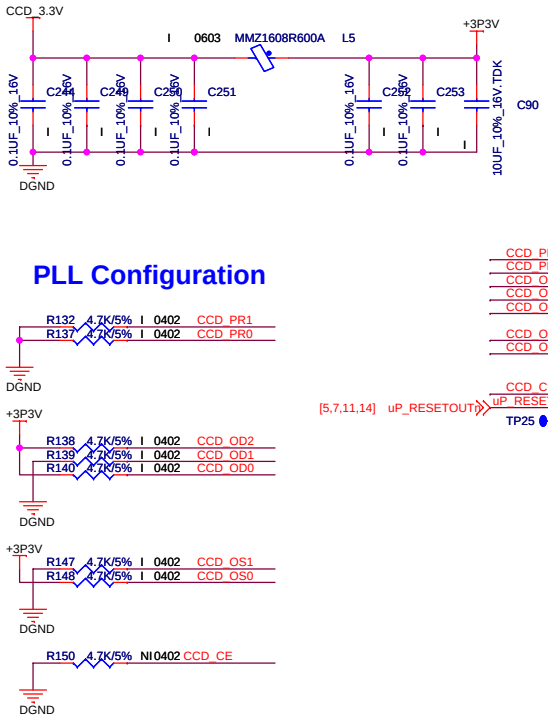
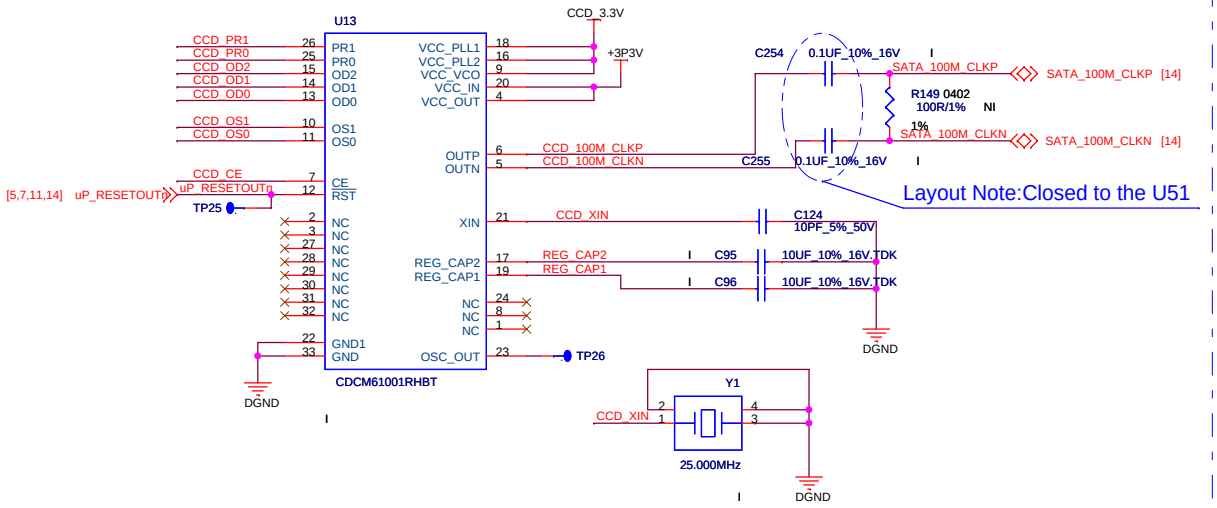
SATA PLL

PLL Configuration

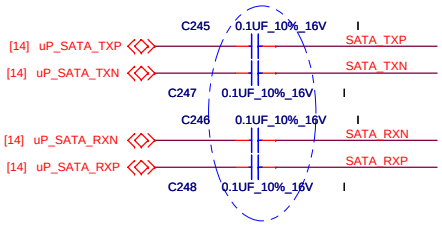




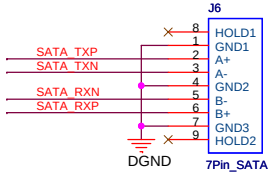
Layout Note:Closed to the U51

SATA Connector

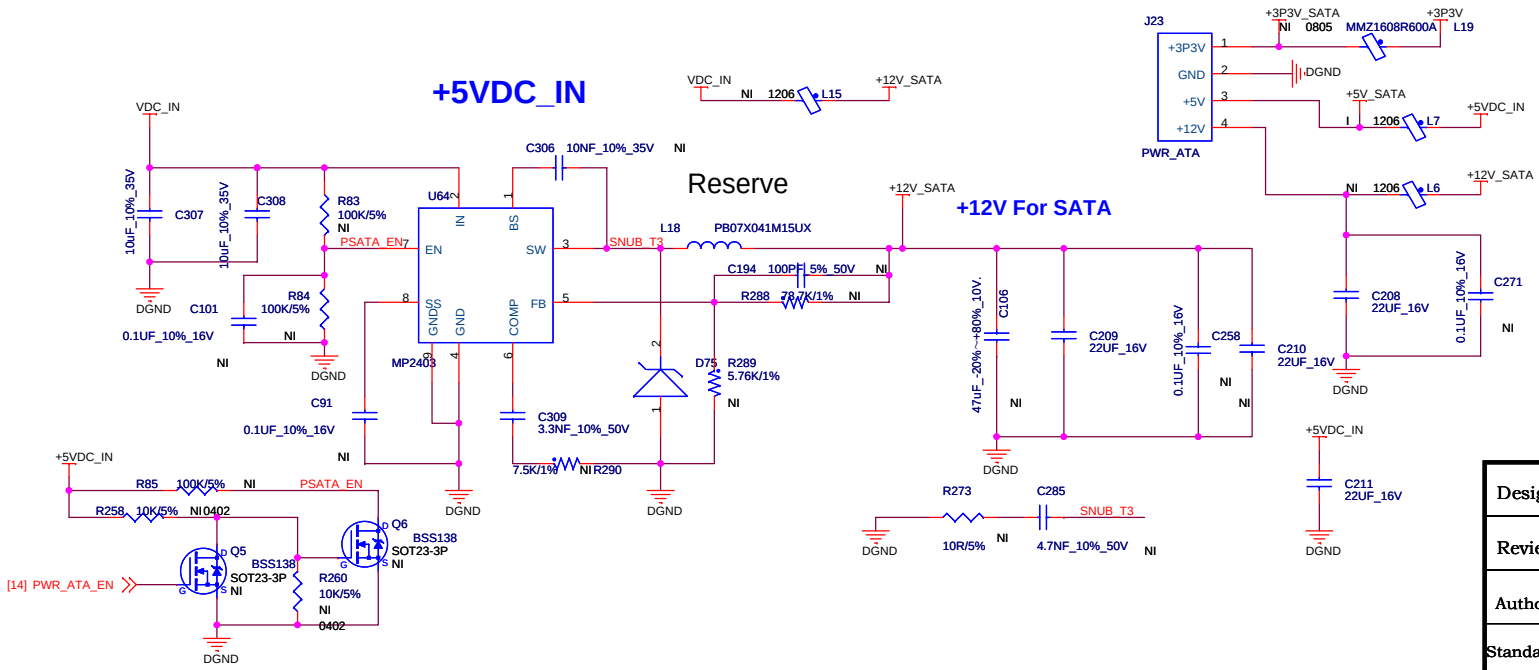
Design Note:
Please place the AC coulping cap close to the SATA Connector .

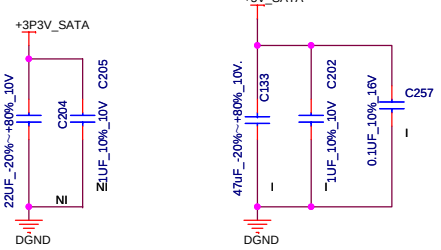


Design Note:
SATA_TXP/N and SATA_RXP/N are Differential pairs that should be routed with 100 Ohm Differential impedence over solidground plane.



+5VDC_IN





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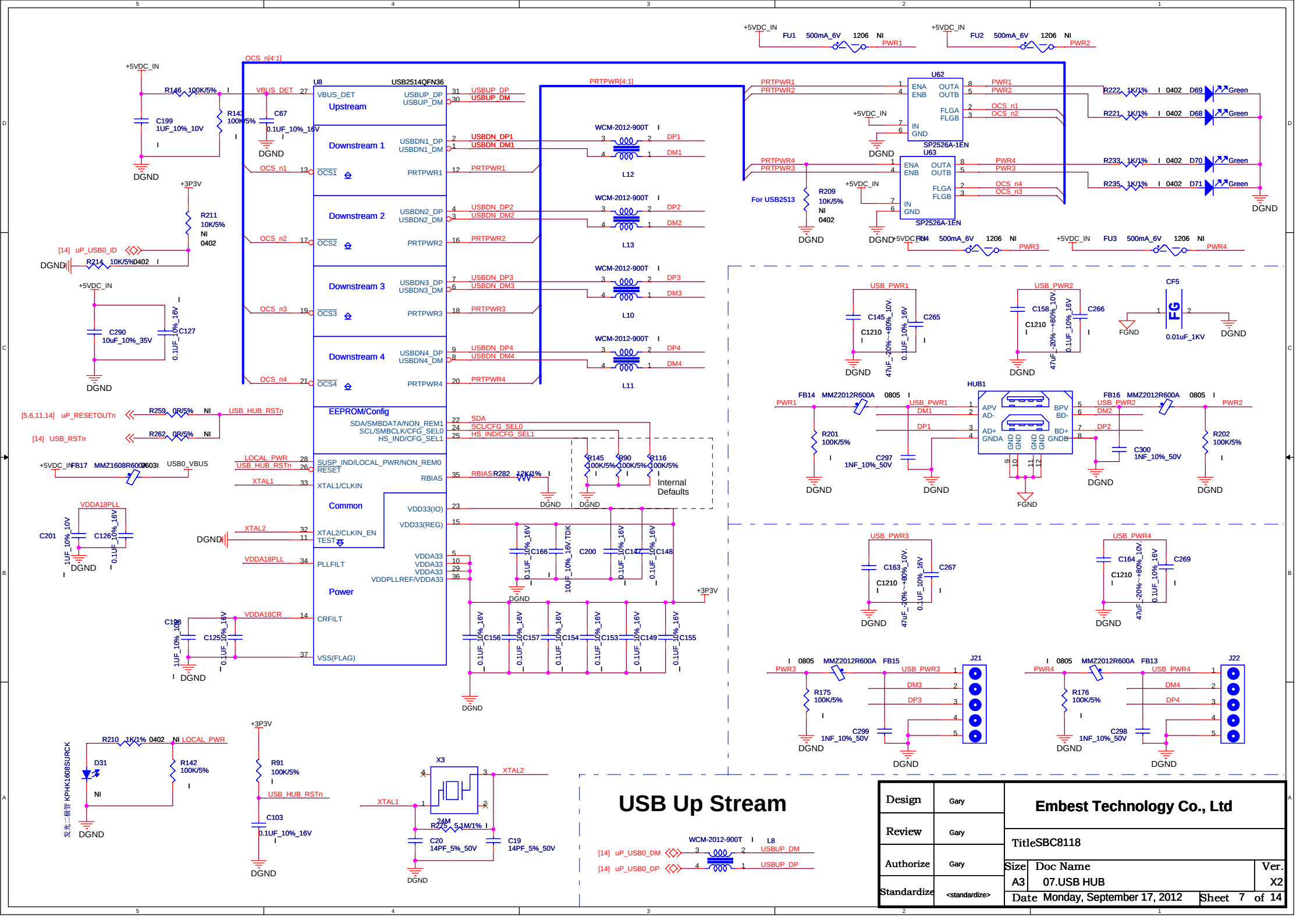
USB Up Stream
U8
USB2514QFN36
Upstream
Downstream 1
Downstream 2
Downstream 3
Downstream 4
EEPROM/Config
Common
Power
OCS_n[4:1]
PRTPWR[4:1]
U62
U63
SP2526A-1EN
For USB2513
WCM-2012-900T
L12
L13
L10
L11
L8
HUB1
J21
J22
X3
24M
Internal Defaults
Design Gary
Review Gary
Authorize Gary
Standardize <standardize>
Embest Technology Co., Ltd
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Ver. X2
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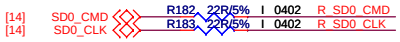
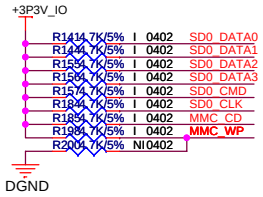
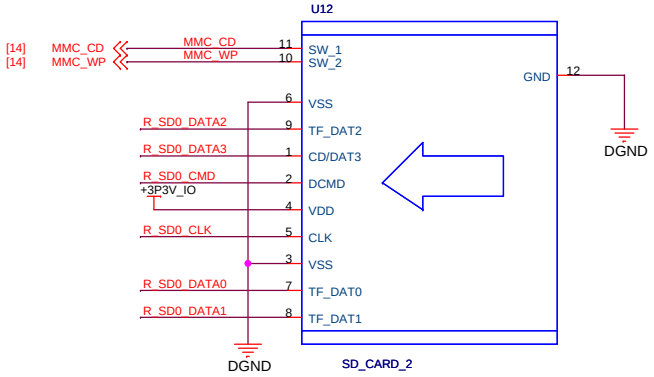
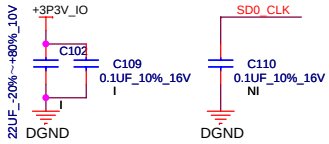
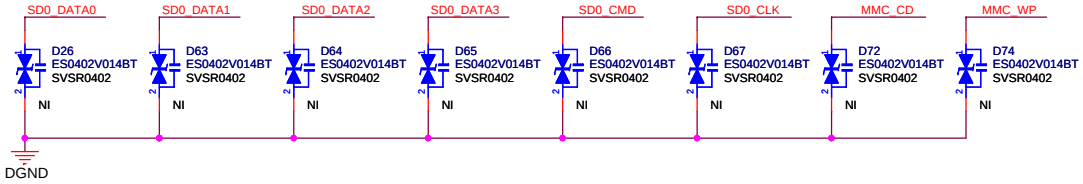
SD Card











Design	Gary	Embest Technology Co., Ltd	
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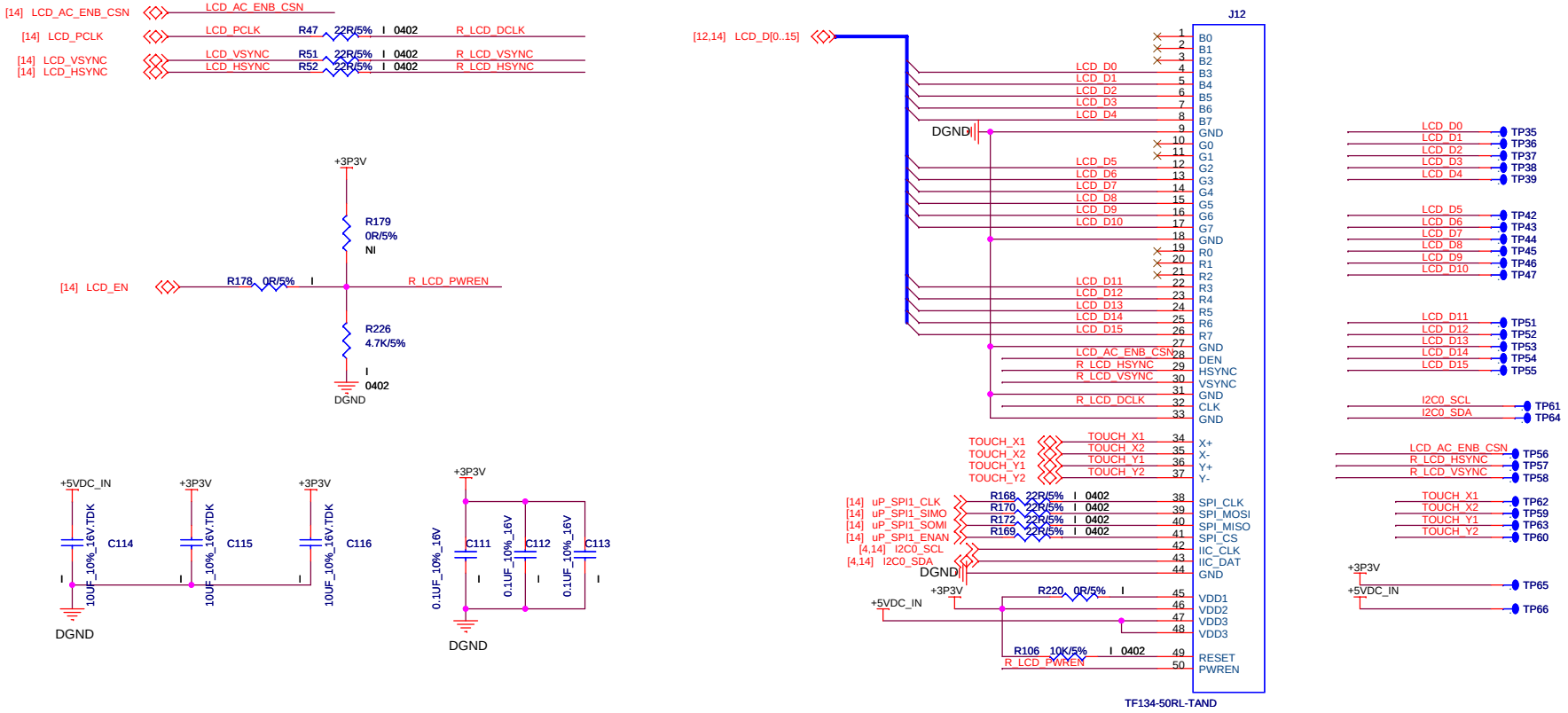
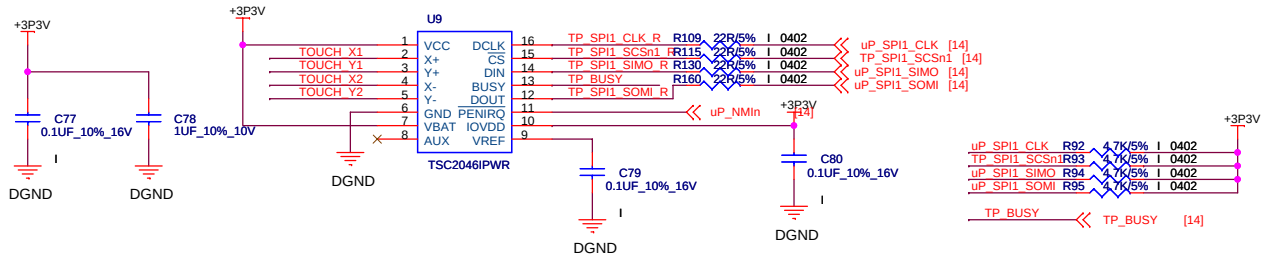
LCD Interface



Touch Screen Controller



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Review	Gary	TitleSBC8118	
Authorize	Gary	Size A3	Doc Name 10.LCD / Ver. X2
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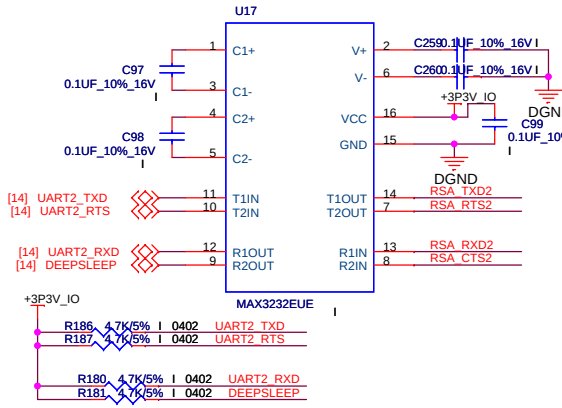
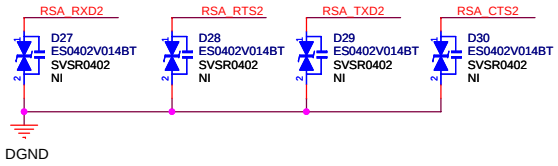
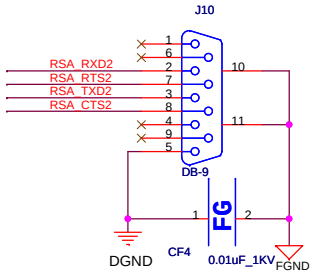
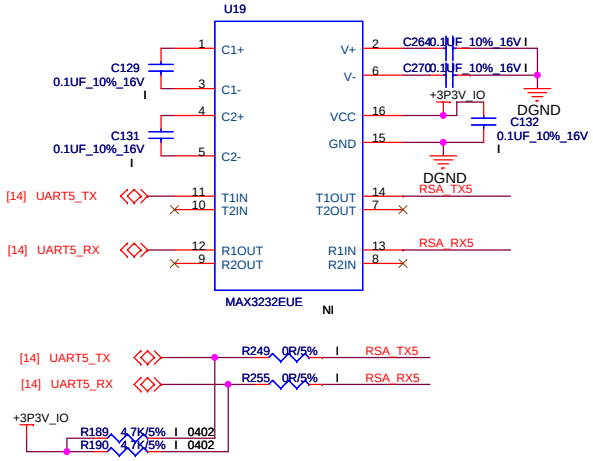
Seaial Output

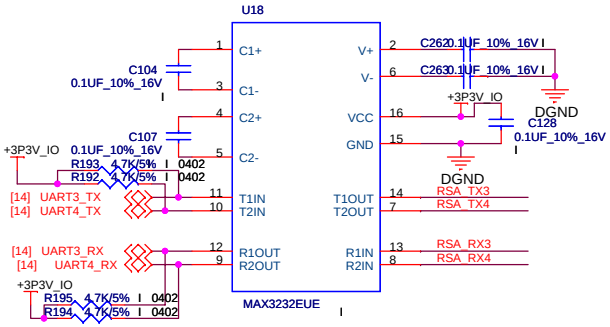


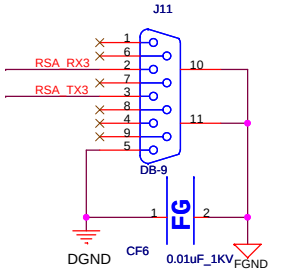


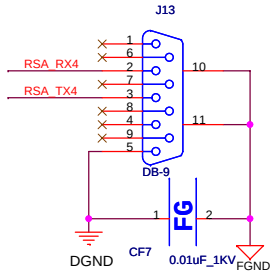
PRU Function

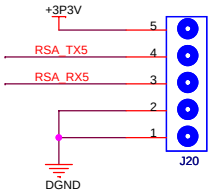


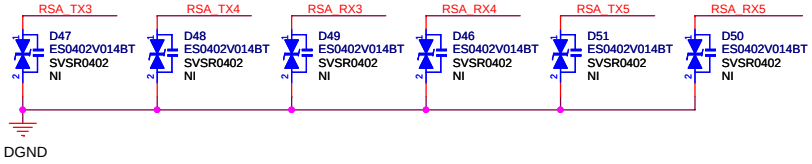




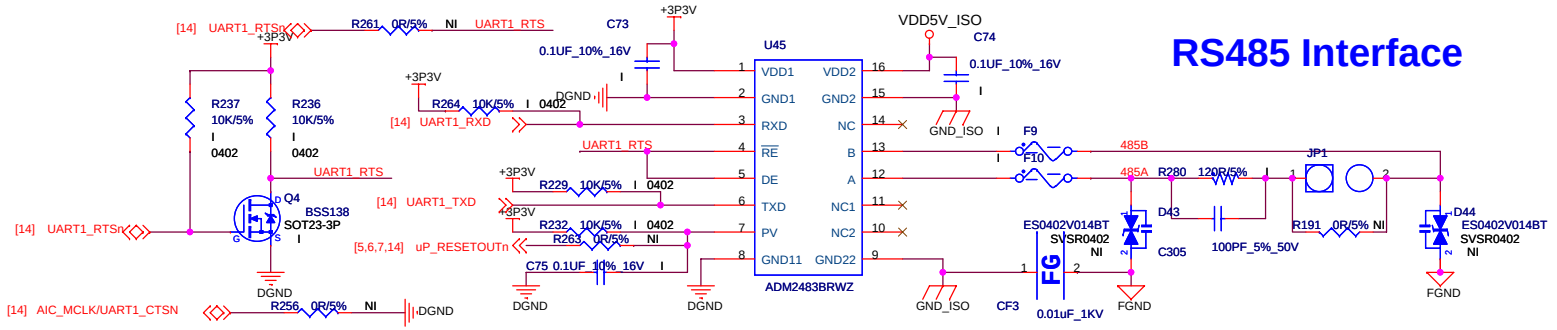


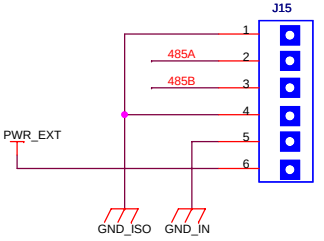




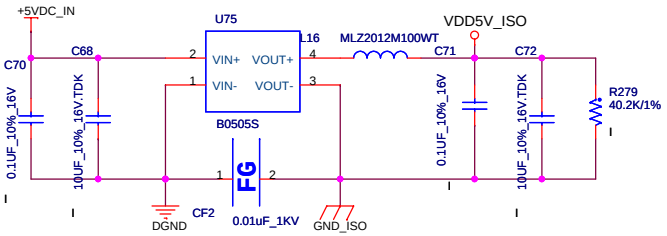


RS485 Interface





+5V DC Isolation



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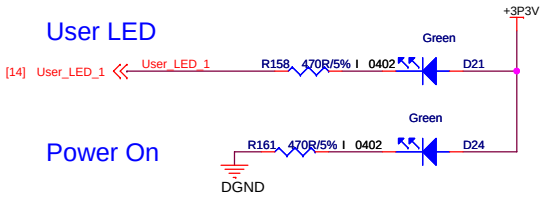
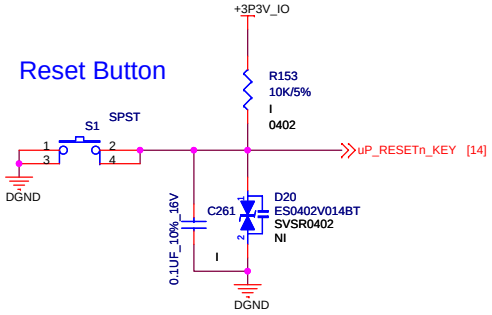
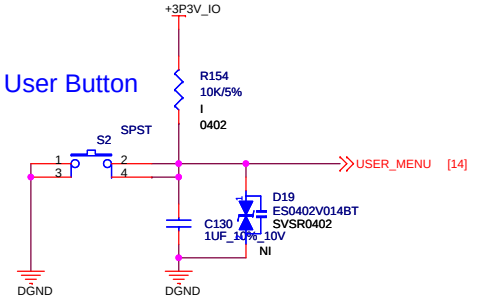
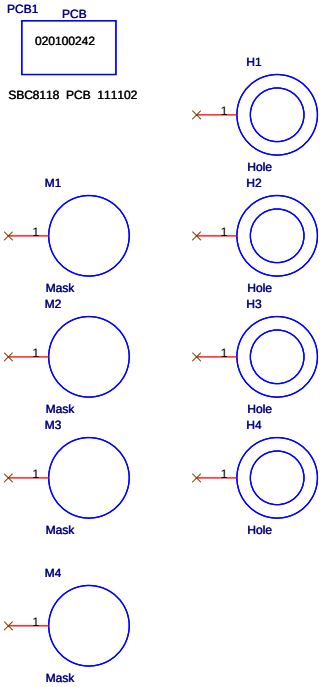
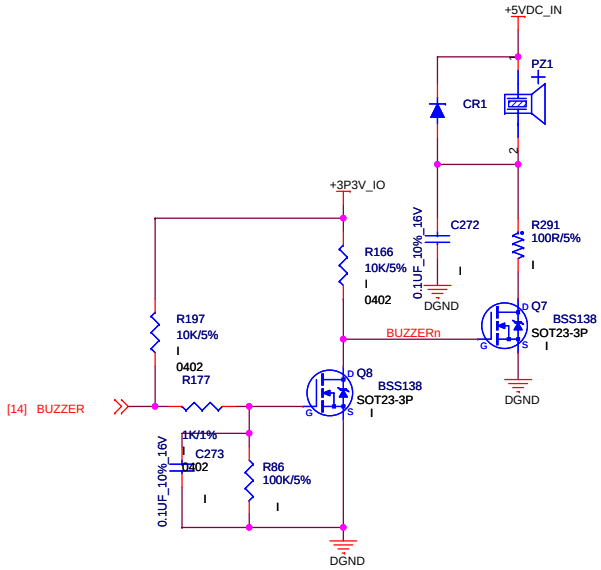


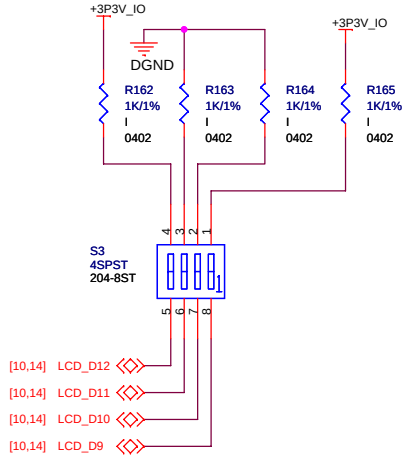








BOOT MODE



A default boot mode has been defined by pulling all boot pins (BOOT[0:7]) to a default state on the SOM. The default boot mode is SPI1 Flash. Other boot modes can be selected as follows:

	Boot Mode	Electrical/Software State BOOT[7:0]		DIP Switch Setting – S7[5:8]			
				BOOT[4]	BOOT[3]	BOOT[2]	BOOT[1]
		Binary	Hex	S7:8	S7:7	S7:6	S7:5
	NOR EMIFA	0000 0010	02	OFF	ON	ON	ON
	NAND-8 EMIFA	0000 1110	0E	OFF	OFF	OFF	ON
	SPI0 Flash	0000 1010	0A	OFF	OFF	ON	ON
Default	SPI1 Flash	0000 1100	0C	OFF	OFF	OFF	OFF
	UART0	0001 0110	16	ON	ON	OFF	ON
	EMU Debug	0001 1110	1E	ON	OFF	OFF	ON

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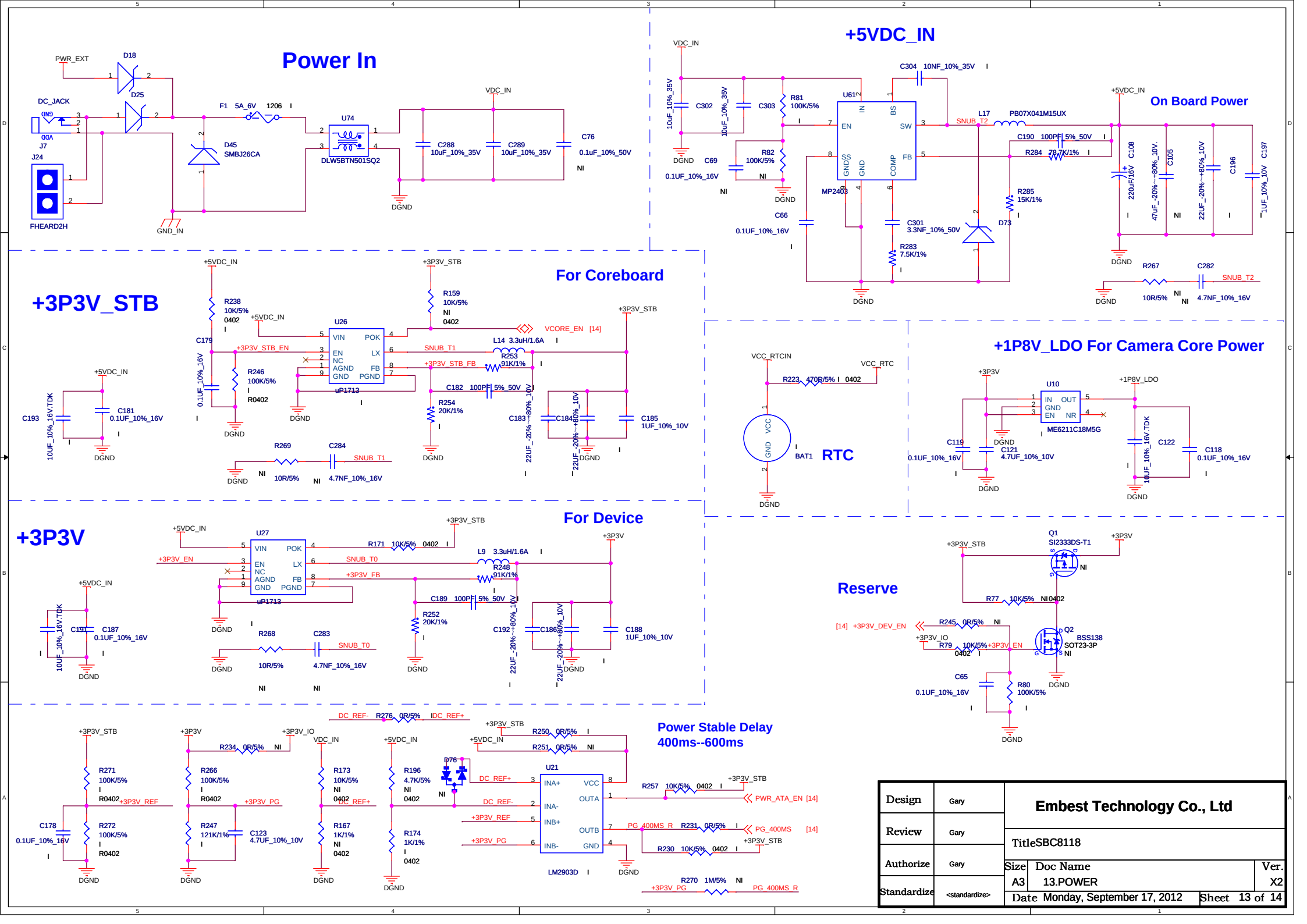
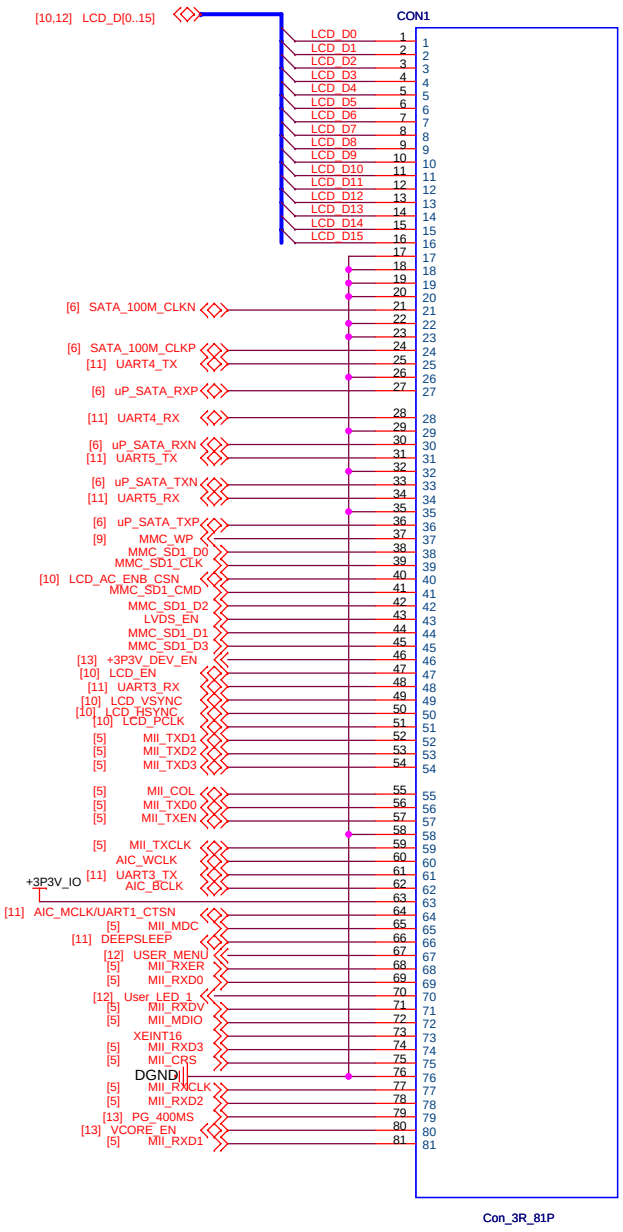
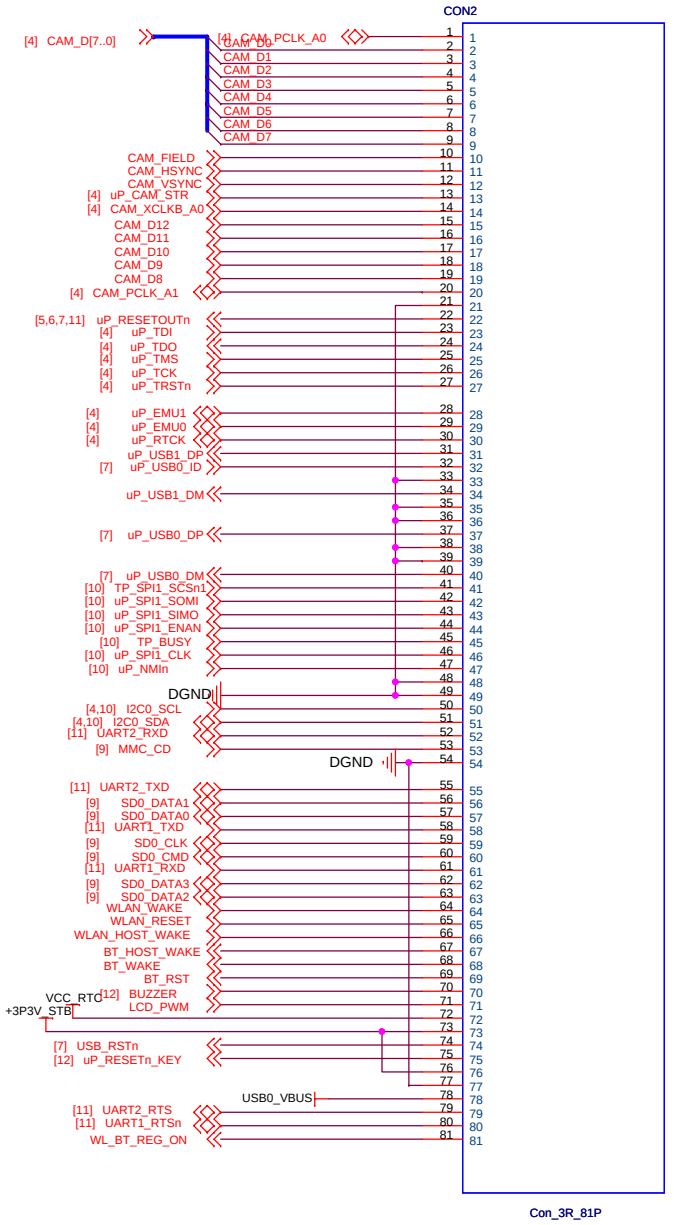

Power In
PWR_EXT
D18
D25
DC_JACK
J7
J24
FHEARD2H
F1 5A_6V 1206
D45 SMBJ26CA
GND_IN
U74
DLW5BTN501SQ2
VDC_IN
C288 10uF_10%_35V
C289 10uF_10%_35V
C76 0.1uF_10%_50V
NI
DGND
+5VDC_IN
VDC_IN
C302 10uF_10%_35V
C303 10uF_10%_35V
R81 100K/5%
R82 100K/5%
C69 0.1UF_10%_16V
U61
MP2403
C304 10NF_10%_35V
L17 PB07X041M15UX
SNUB_T2
C190 100PF_5%_50V
R284 78.7K/1%
R285 15K/1%
D73
C301 3.3NF_10%_50V
R283 7.5K/1%
C66 0.1UF_10%_16V
On Board Power
C108 220uF/16V
C105 47uF_-20%~+80%_10V
C196 22UF_-20%~+80%_10V
C197 1UF_10%_10V
R267 10R/5%
C282 4.7NF_10%_16V
+3P3V_STB
For Coreboard
R238 10K/5%
R159 10K/5%
U26
VIN POK
EN LX
NC
AGND FB
GND PGND
uP1713
+3P3V_STB_EN
VCORE_EN [14]
SNUB_T1
L14 3.3uH/1.6A
R253 91K/1%
+3P3V_STB_FB
C182 100PF_5%_50V
R254 20K/1%
C179 0.1UF_10%_16V
R246 100K/5%
R0402
C181 0.1UF_10%_16V
C193 10UF_10%_16V.TDK
C183 22UF_-20%~+80%_10V
C184 22UF_-20%~+80%_10V
C185 1UF_10%_10V
R269 10R/5%
C284 4.7NF_10%_16V
VCC_RTCIN
VCC_RTC
R223 470R/5% 0402
VCC
GND
BAT1
RTC
+1P8V_LDO For Camera Core Power
+3P3V
U10
IN OUT
GND
EN NR
ME6211C18M5G
+1P8V_LDO
C119 0.1UF_10%_16V
C121 4.7UF_10%_10V
C122 10UF_10%_16V.TDK
C118 0.1UF_10%_16V
+3P3V
For Device
U27
+3P3V_EN
SNUB_T0
+3P3V_FB
L9 3.3uH/1.6A
R248 91K/1%
R171 10K/5% 0402
C189 100PF_5%_50V
R252 20K/1%
C191 10UF_10%_16V.TDK
C187 0.1UF_10%_16V
C192 22UF_-20%~+80%_10V
C186 22UF_-20%~+80%_10V
C188 1UF_10%_10V
R268 10R/5%
C283 4.7NF_10%_16V
Reserve
Q1 SI2333DS-T1
R77 10K/5% 0402
[14] +3P3V_DEV_EN
R245 0R/5%
+3P3V_IO
R79 10K/5%
Q2 BSS138 SOT23-3P
C65 0.1UF_10%_16V
R80 100K/5%
Power Stable Delay 400ms--600ms
DC_REF-
R276 0R/5%
DC_REF+
R250 0R/5%
R251 0R/5%
R234 0R/5%
R271 100K/5%
R0402
C178 0.1UF_10%_16V
R272 100K/5%
R266 100K/5%
R247 121K/1%
C123 4.7UF_10%_10V
R173 10K/5%
R167 1K/1%
R196 4.7K/5%
R174 1K/1%
D76
U21
INA+ VCC
INA-
INB+
INB-
OUTA
OUTB
GND
LM2903D
R257 10K/5% 0402
PWR_ATA_EN [14]
PG_400MS_R
R231 0R/5%
PG_400MS [14]
R230 10K/5% 0402
R270 1M/5%
+3P3V_REF
+3P3V_PG
Design Gary
Review Gary
Authorize Gary
Standardize <standardize>
Embest Technology Co., Ltd
TitleSBC8118
Size A3
Doc Name 13.POWER
Ver. X2
Date Monday, September 17, 2012
Sheet 13 of 14





Design	Gary	Embest Technology Co., Ltd	
Review	Gary	TitleSBC8118	
Authorize	Gary	Size: A3	Doc Name: 14.CoreBoard B2B — Ver.: X2
Standardize	<standardize>	Date: Monday, September 17, 2012	Sheet: 14 of 14