

Rlot board

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Design	XuZHH	Embest Technology Co.,Ltd.			
Review	ZHDP				
Authorize	Qunsun	TitleRlot Board			
Standardize	<standardize>	Size	Doc Name		Ver.
		A3	01.CONVER PAGE		130701
		Date	Friday, December 13, 2013	Sheet	01 of 20

Schematic History

2013-07-19

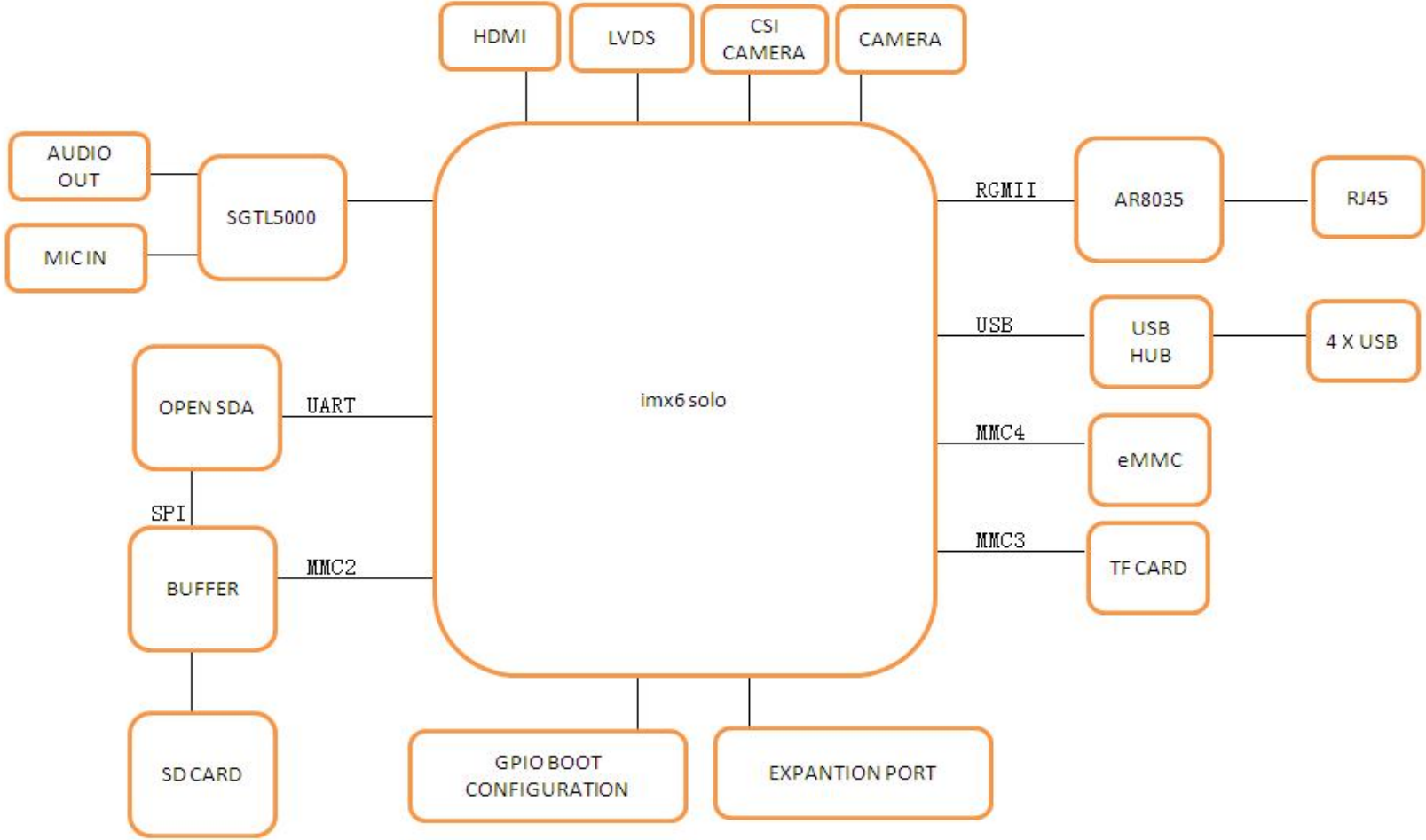
- 1.update all the parts reference to fix drc error
- 2.change bus SDA_SD4_* to SDA_SD2_* on PAGE(15)
- 3.add I2C2_SCL/SDA connect to PMIC (PAGE05)
- 4.remove TPS3808G33DBVT (PAGE18),
use PMIC internal reset for IMX6(PAGE05)

2013-08-01

- 1.Separate RJ45+Dual USB

Design	XuZHH	Embest Technology Co.,Ltd.			
Review	ZHDP				
		TitleRlot Board			
Authorize	Qunsun	Size	Doc Name		Ver.
		A3	02.Schematic History		130701
Standardize	<standardize>	Date	Friday, December 13, 2013		Sheet 02 of 20

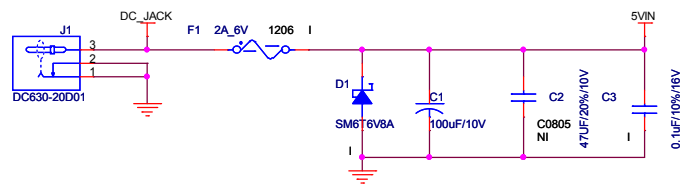
SYSTEM BLOCK



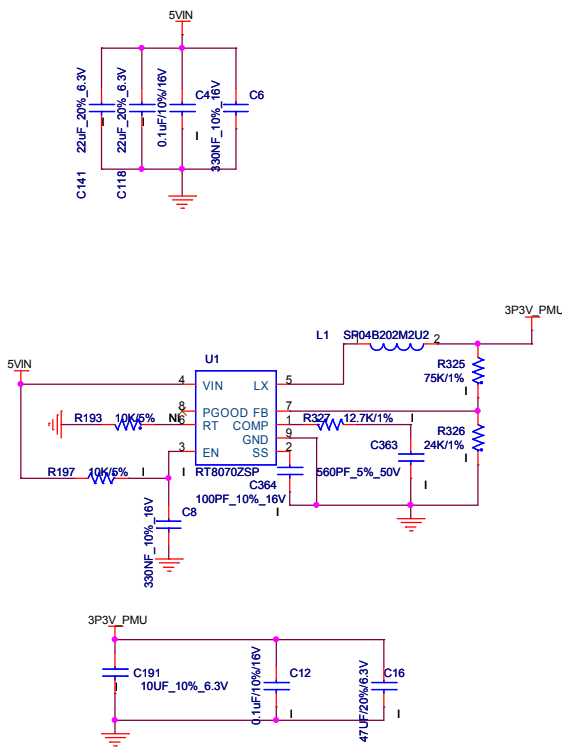
PCB1 PCB
1001001000234

Design	xuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRlot Board		
Authorize	Qunsun	Size	Doc Name	Ver.
Standardize	<standardize>	A3	03.SYSTEM BLOCK	130701
		Date	Friday, December 13, 2013	Sheet 03 of 20

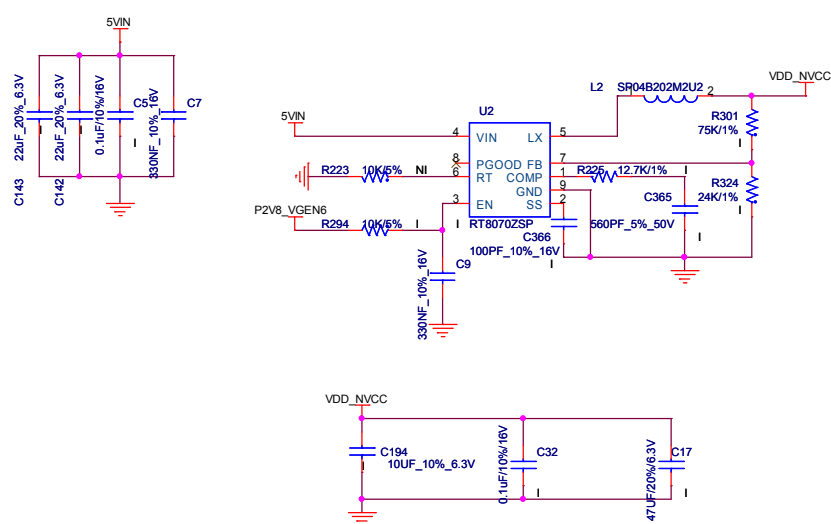
Main Power



PMIC Power Feed 3.5 A max



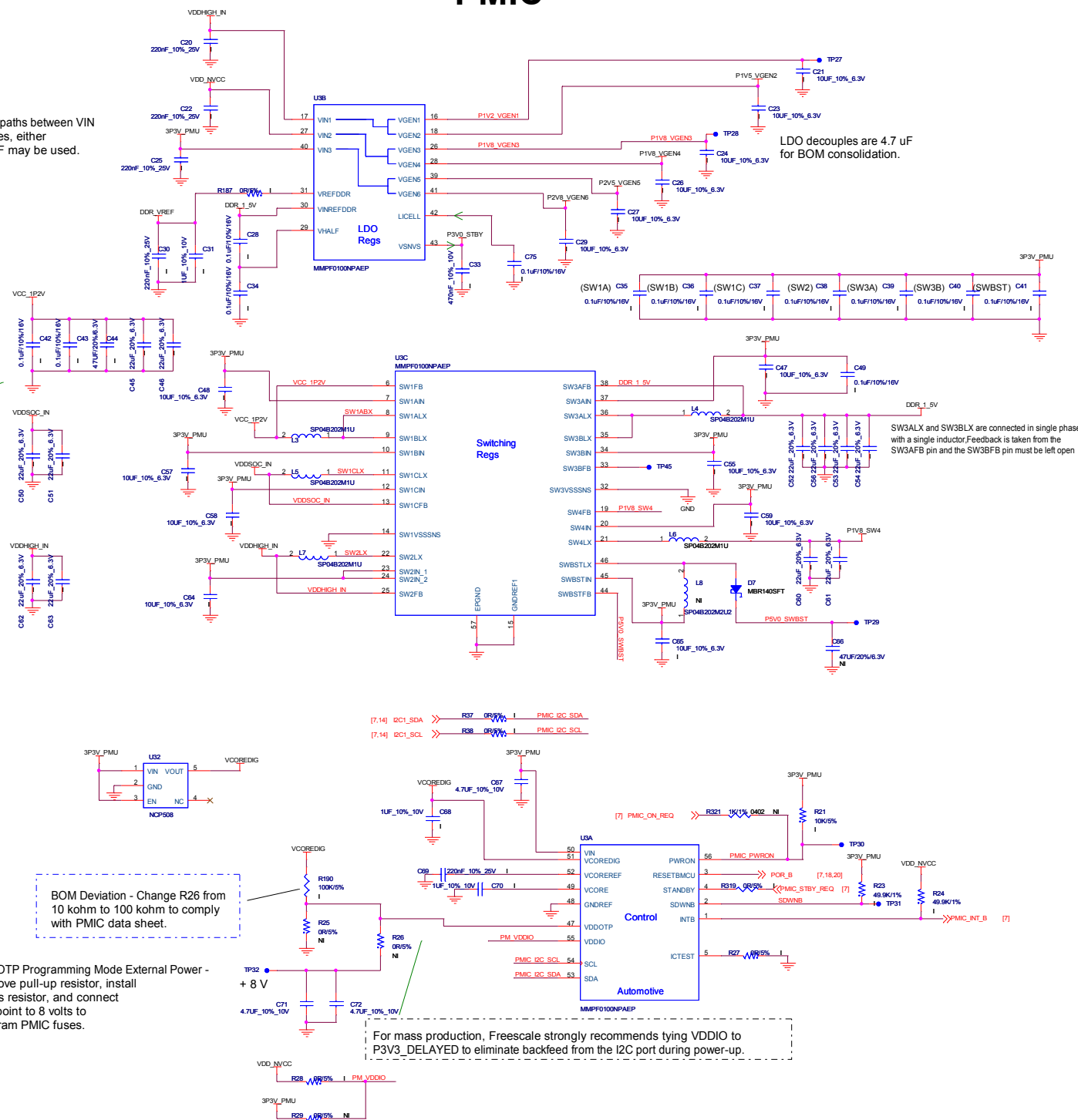
Peripheral Power Supply 3.5 A max



Design	xuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRlot Board		
Authorize	Qunsun	Size A3	Doc Name 04 MAIN POWER	Ver. 130701
Standardize	<standardize>	Date Friday, December 13, 2013	Sheet 04 of 20	

PMIC

With low-inductive paths between VIN the voltage sources, either 0.22 uF or 0.47 uF may be used.



Peripheral Power Rails

Voltage (V)	Rail Name	Block	Power Source	Generate By	Current Capability (A)
12	VBAT	MLB	Wall Supply	MB	5.5
5	P5V0_DELAYED	Para LCD	Main Power	MB or Jack	
		LVDS LCD			
		HDMI			
		MIPI			
	P5V0_OTG_VBUS	USB			0.5
P5V0_H1_VBUS	USB	switcher	MB	0.8	
3.3	P3V3_DELAYED	NAND Flash	switcher	LT3680	3.5
		SD Card			
		NOR Flash			
		HDMI			
		LVDS LCD			
		Ethernet			
		UART			
		MIPI			
		Mini PCIE			
		MLB (MOST)			
3.0	P3V0_VDD_USB	USB	VDDUSB_CAP	iMX	-
2.8	P2V8_VGEN6	MIPI	VGEN6	PMIC	0.2
1.8	P1V8_SW4	MIPI	SW4	PMIC	1.0
	P1V8_VGEN4	SD Card	VGEN4	PMIC	0.35
1.5	P1V5_DDR_SW3	DDR	SW3A/B	PMIC	2.5
	P1V5_VGEN2	Mini PCIE	VGEN2	PMIC	0.25
1.5	ETH_VDDIO_REG	Ethernet	PHY - on-chip	AR8031	-
0.75	POV75_REFDDR	DDR	VREFDDR	PMIC	0.01

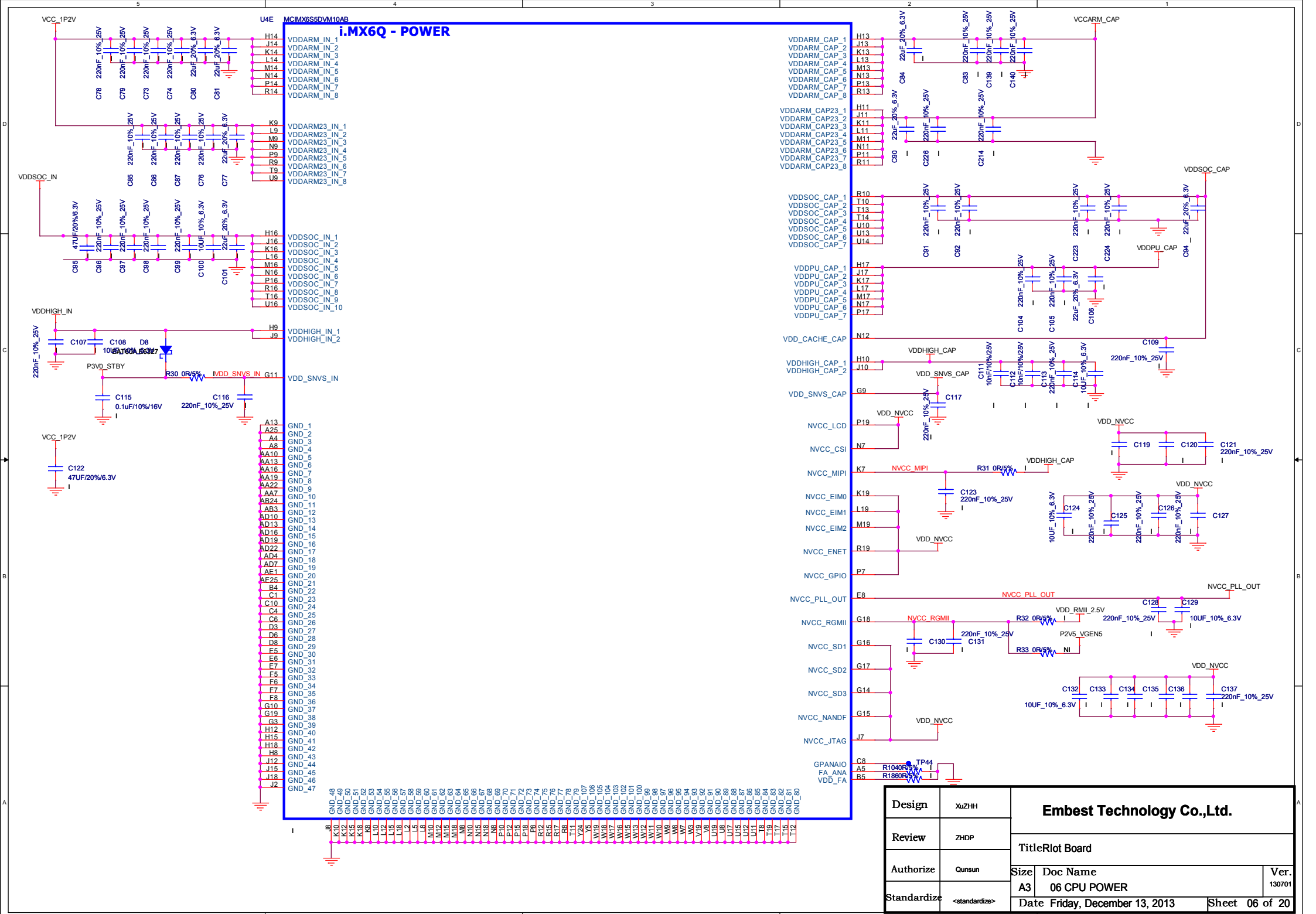
MB = Main board 26662

PMIC Output Rails

Regulator	Voltage (V)	Power-Up Sequence	Load
VS_NVS	3	0	VDD_SNVS_IN
SW1A/B	1.375	1	VDDARM_IN
SW1C	1.375	1	VDDSOC_IN
SW2	3	2	VDDHIGH_IN
VGEN2	1.5	2	mini PCIe connector
SW3A/B	1.5	3	NVCC_DRAM, NVCC_RGMII (option)
SW4	1.8	3	MIPI connector
VGEN4	1.8	3	NVCC_SD3
VGEN6	2.8	3	3V3_DELAYED enable, MIPI conn
VREFDDR	0.75	3	DRAM_VREF
VGEN5	2.5	3	Pwr LED & 5V0_DELAYED enable
SWBST	0	N/A	Not used
VGEN1	0	N/A	Not used
VGEN3	0	N/A	Not used

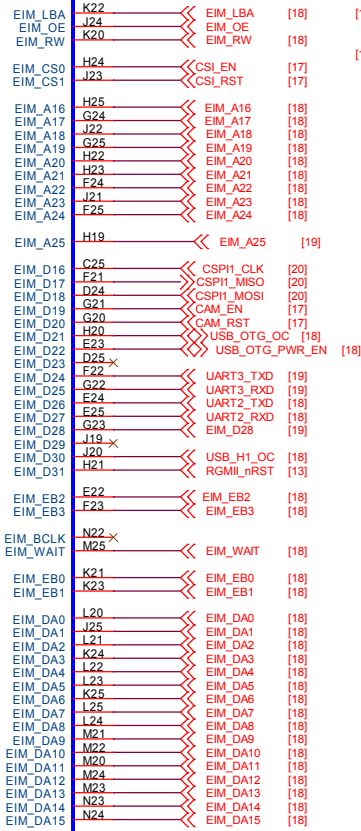
SW1A/B = 1.375 V for boot-up at ~800 MHz.
Recommend that software increase SW1A/B
to 1.425 V for 1 GHz operation.

Design	XJ2FH	Embest Technology Co.,Ltd.		
Review	ZKOP			
Authorize	Qiansun	TitleRiot Board		
Standardize	<standard>	Size	Doc Name	Ver.
		A2	05 PMIC	130701
		Date	Friday, December 13, 2013	Sheet 05 of 20



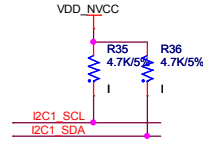
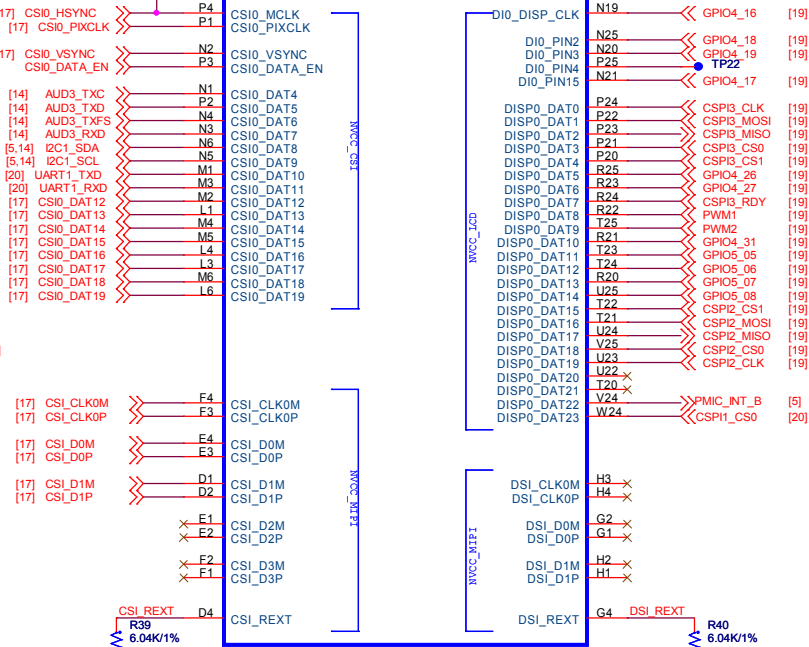
U4A
MCIMX6S5DVM10AB

i.MX6Q - EIM

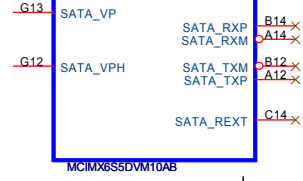


[17] CSI_MCLK

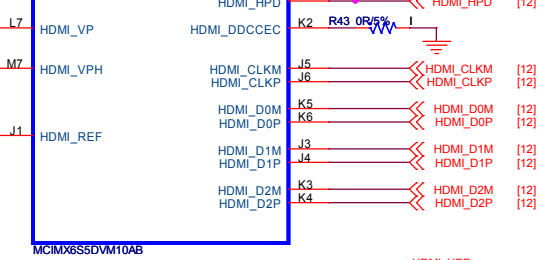
i.MX6Q - DISP; CSI



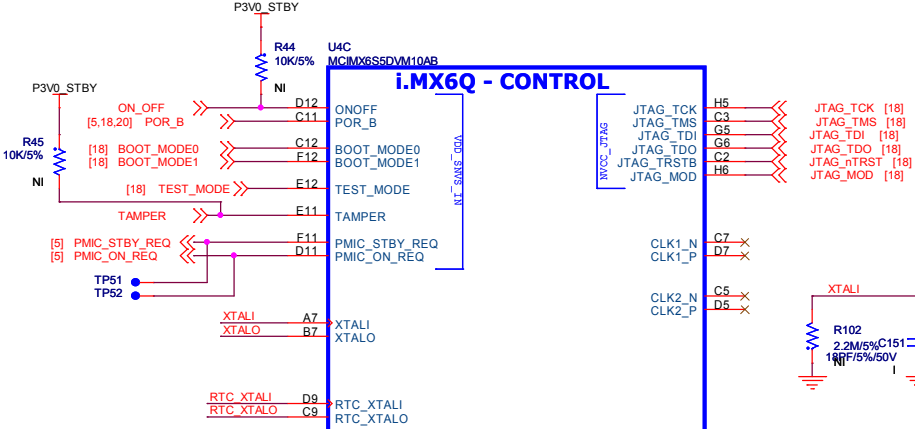
i.MX6Q - SATA



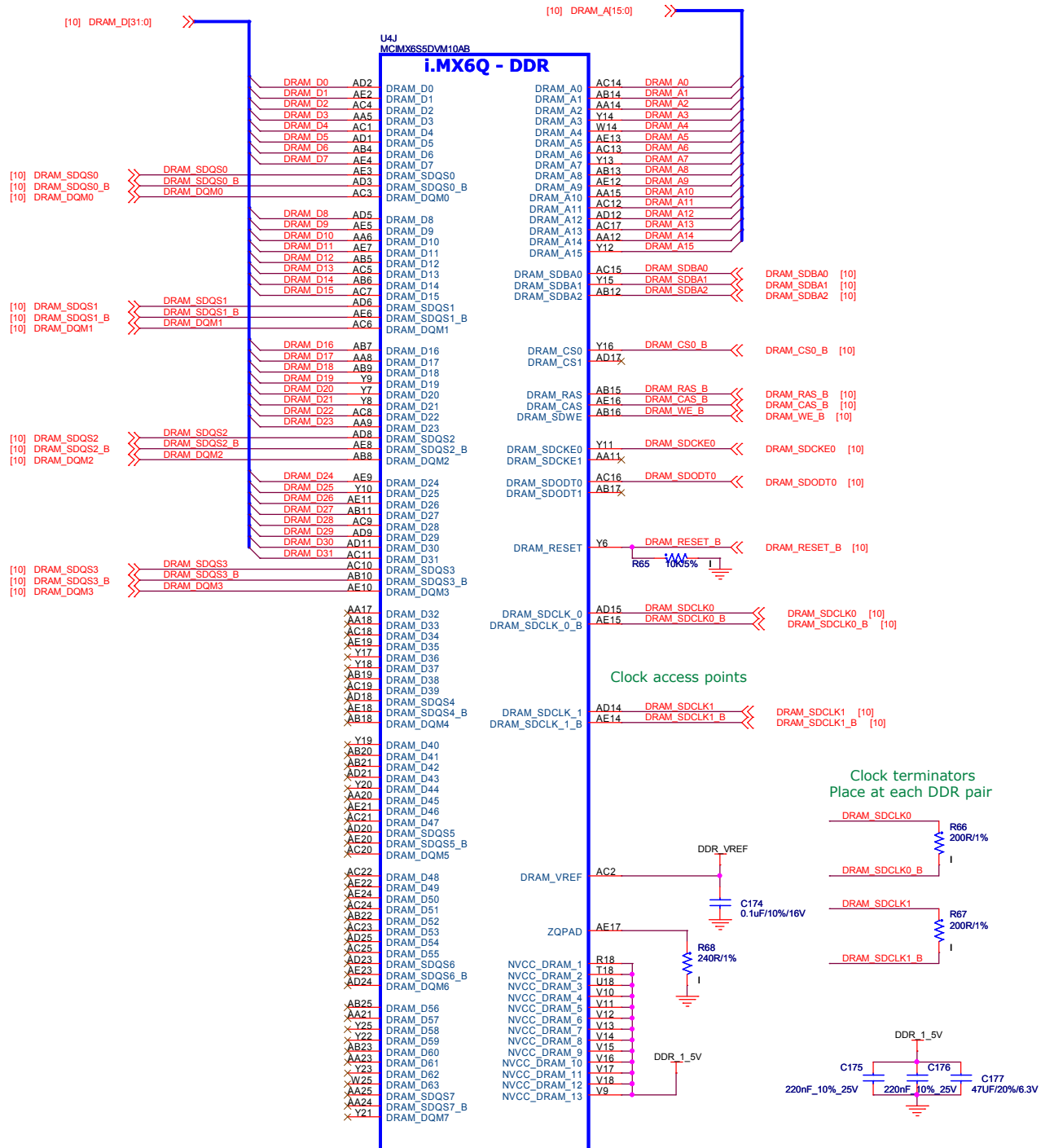
i.MX6Q - HDMI



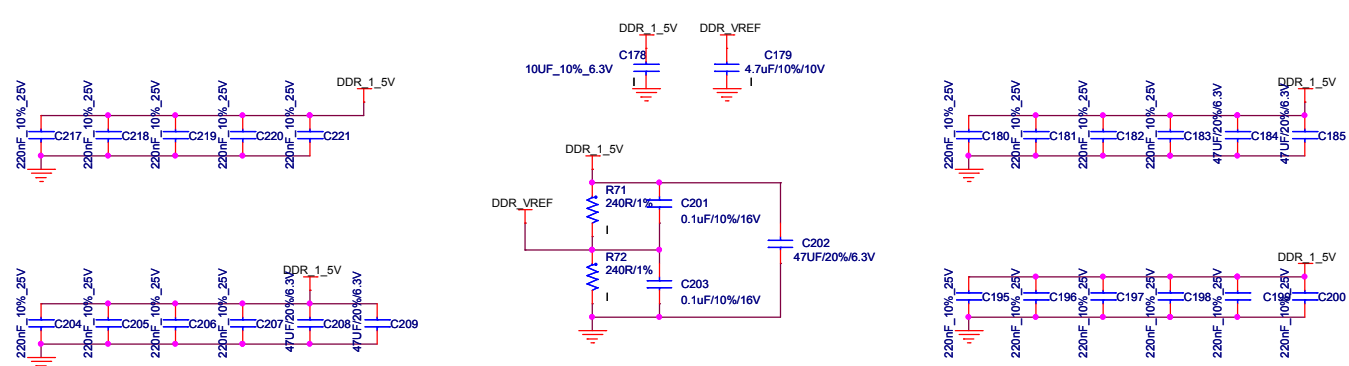
i.MX6Q - CONTROL



Design	XuZHH	Embest Tech Co. LTD		
Review	ZHDP	TitleRiot Board		
Authorize	Qunsun	Size	Doc Name	Ver.
Standardize	<standardize>	A3	07 IMX6Q_SOC_A	130701
		Date	Friday, December 13, 2013	Sheet 07 of 20

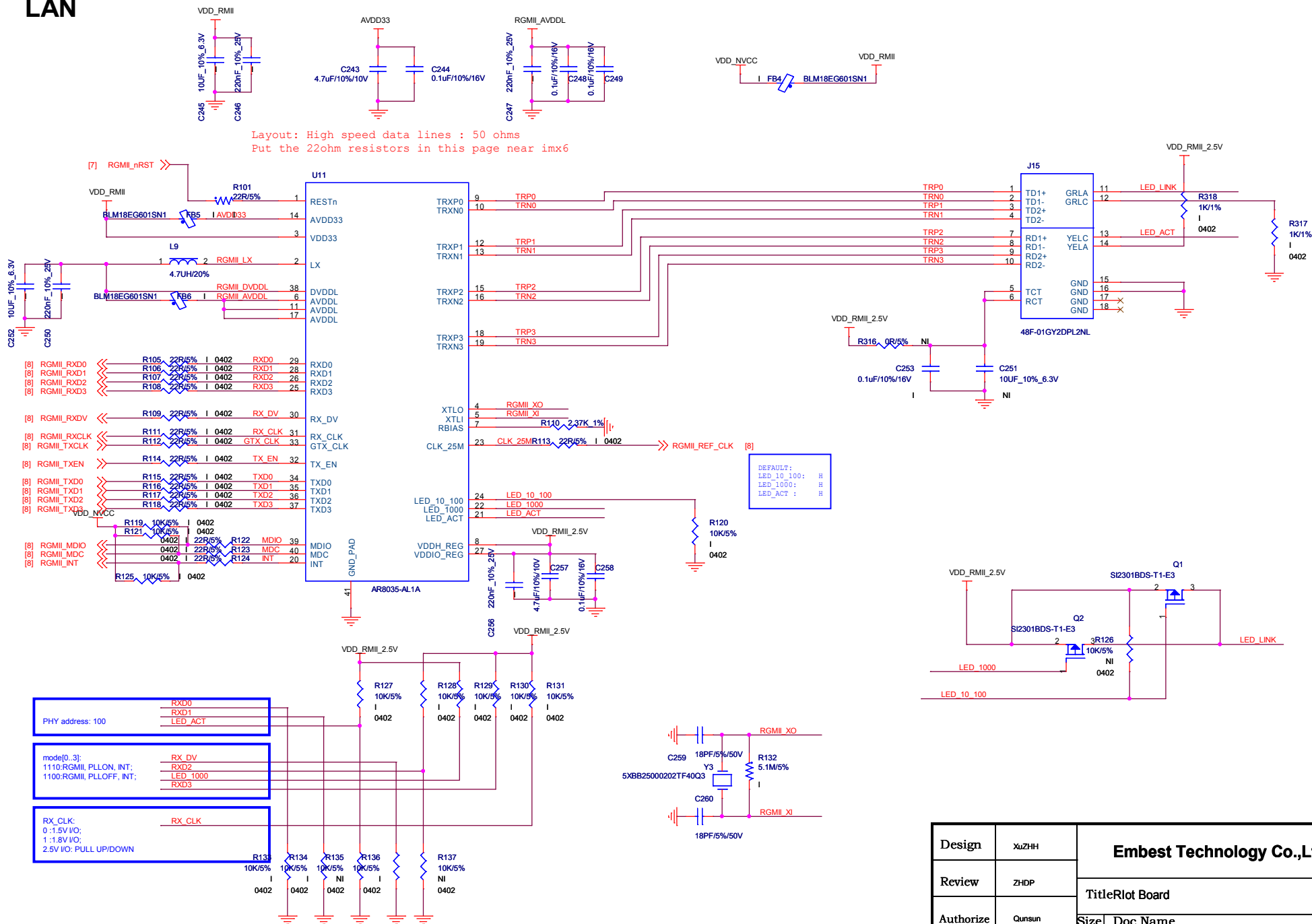


Design	XuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRiot Board		
Authorize	Qunsun	Size A3	Doc Name 09 IMX6Q_SOC_C	Ver. 130701
Standardize	<standardize>	Date Friday, December 13, 2013	Sheet 09 of 20	



Design	XuZHH	Embest Technology Co.,Ltd.			
Review	ZHDP				
Authorize	Qunsun	TitleRlot Board			
Standardize	<standardize>	Size A3	Doc Name 10 DDR3		Ver. 130701
		Date	Friday, December 13, 2013		Sheet 10 of 20

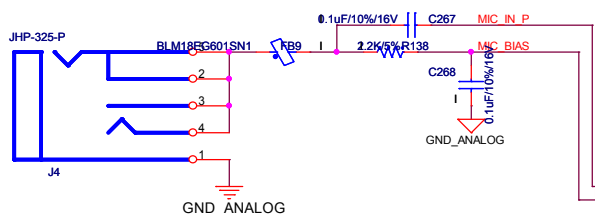
LAN



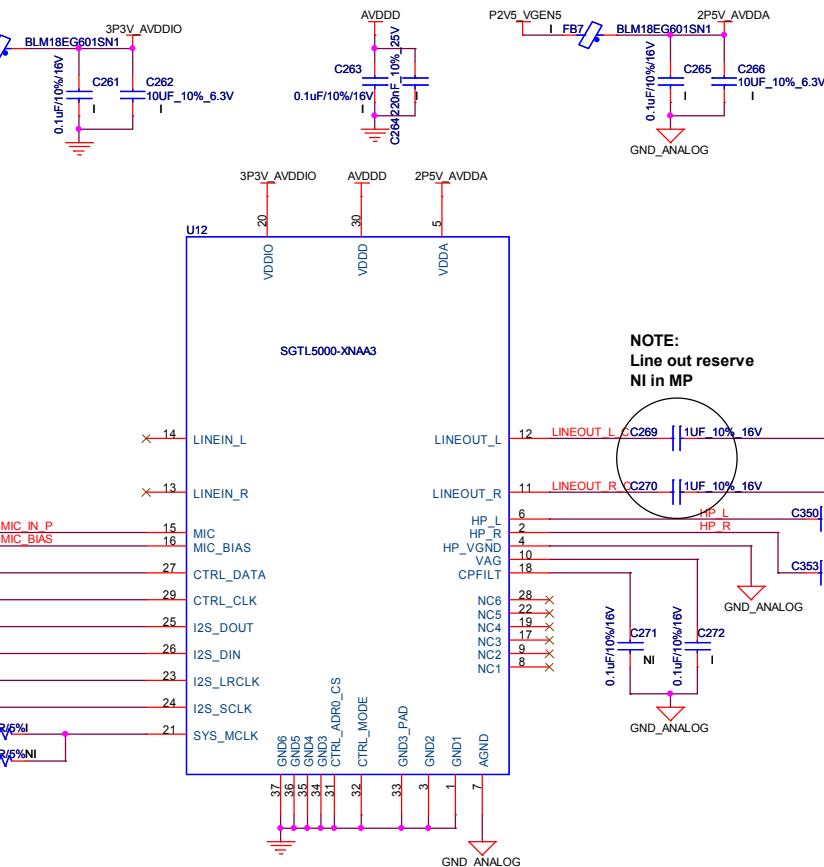
Design	XuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRiot Board		
Authorize	Qunsun	Size	Doc Name	Ver.
Standardize	<standardize>	A3	13 RGMII	130701
		Date	Friday, December 13, 2013	Sheet 13 of 20

AUDIO

MIC IN

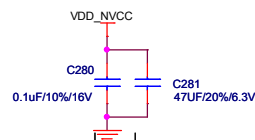
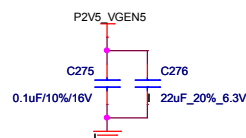
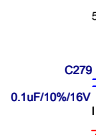
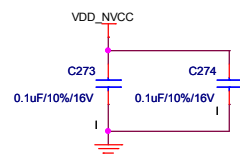
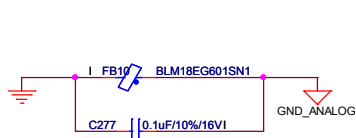
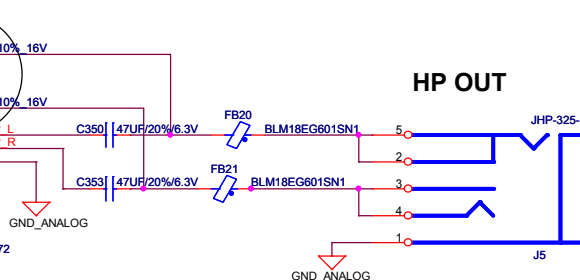


- [5,7] I2C1_SDA >> 27 CTRL_DATA
- [5,7] I2C1_SCL >> 29 CTRL_CLK
- [7] AUD3_RXD >> 25 I2S_DOUT
- [7] AUD3_TXD >> 26 I2S_DIN
- [7] AUD3_TXFS >> 23 I2S_LRCLK
- [7] AUD3_TXC >> 24 I2S_SCLK
- [8,17] CAM_MCLK >> 21 SYS_MCLK
- [8] GPIO_3_CLK >> 21 SYS_MCLK



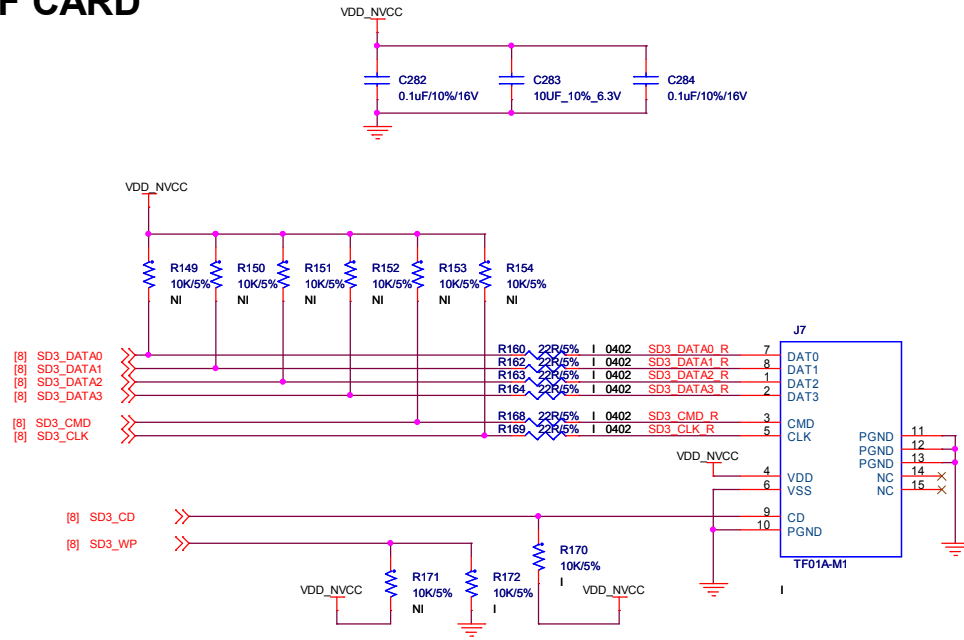
NOTE:
Line out reserve
NI in MP

HP OUT

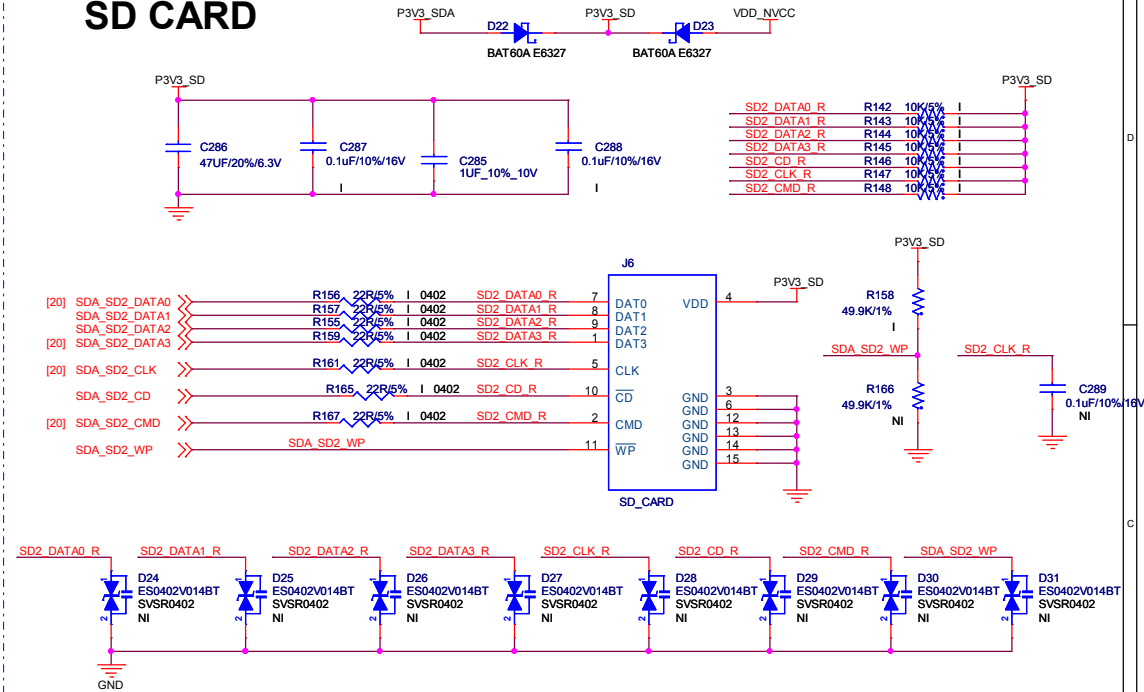


Design	XuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRlot Board		
Authorize	Qunsun	Size	Doc Name	Ver.
Standardize	<standardize>	A3	14 AUDIO	130701
		Date	Friday, December 13, 2013	Sheet 14 of 20

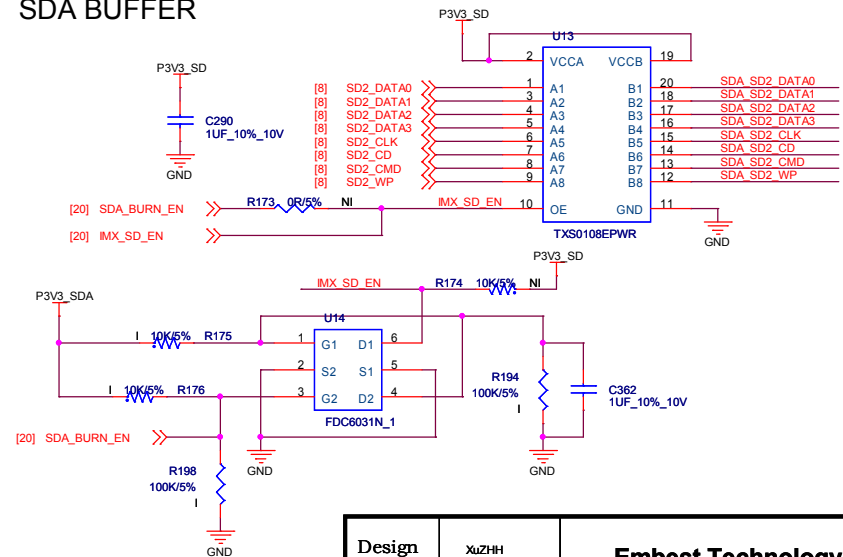
TF CARD



SD CARD

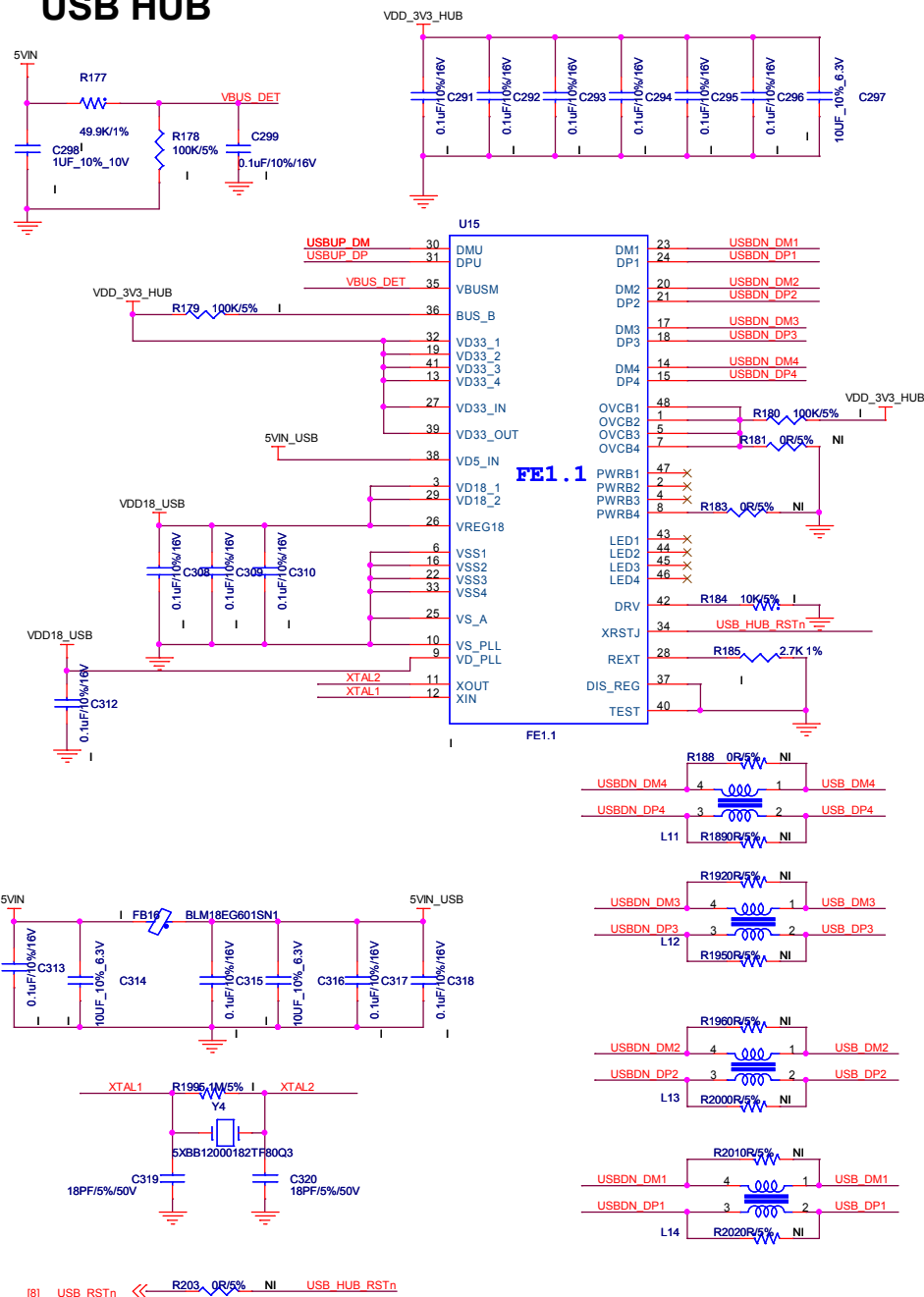


SDA BUFFER

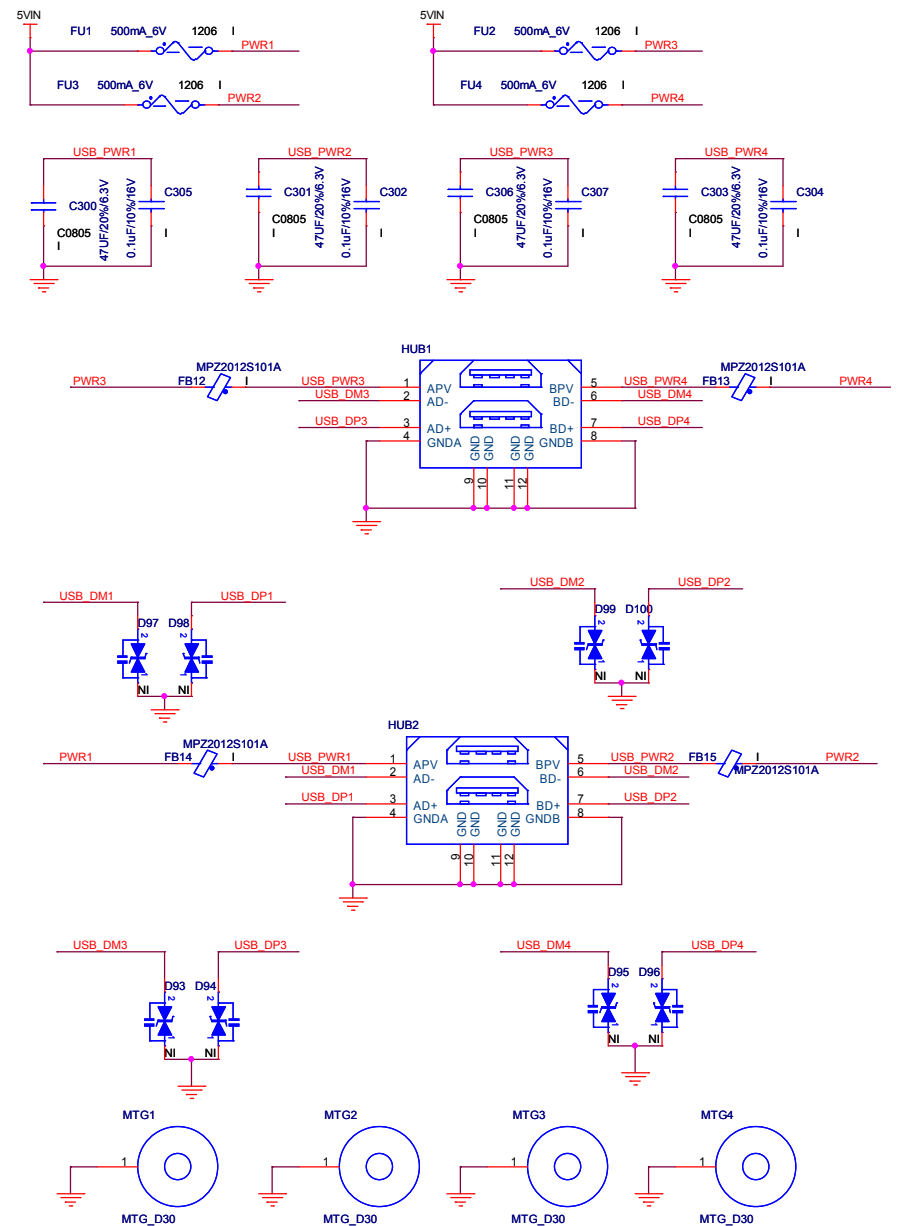


Design	xuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRlot Board		
Authorize	Qunsun	Size	Doc Name	Ver.
Standardize	<standardize>	A3	15 SD/MMC	130701
		Date	Friday, December 13, 2013	Sheet 15 of 20

USB HUB

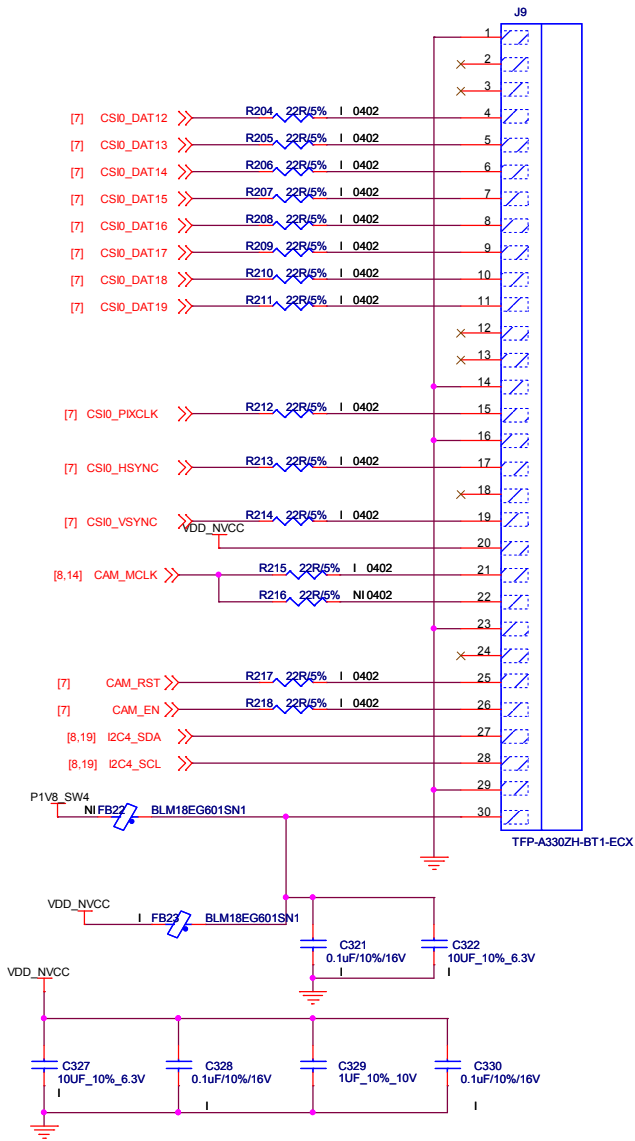


USB Up Stream

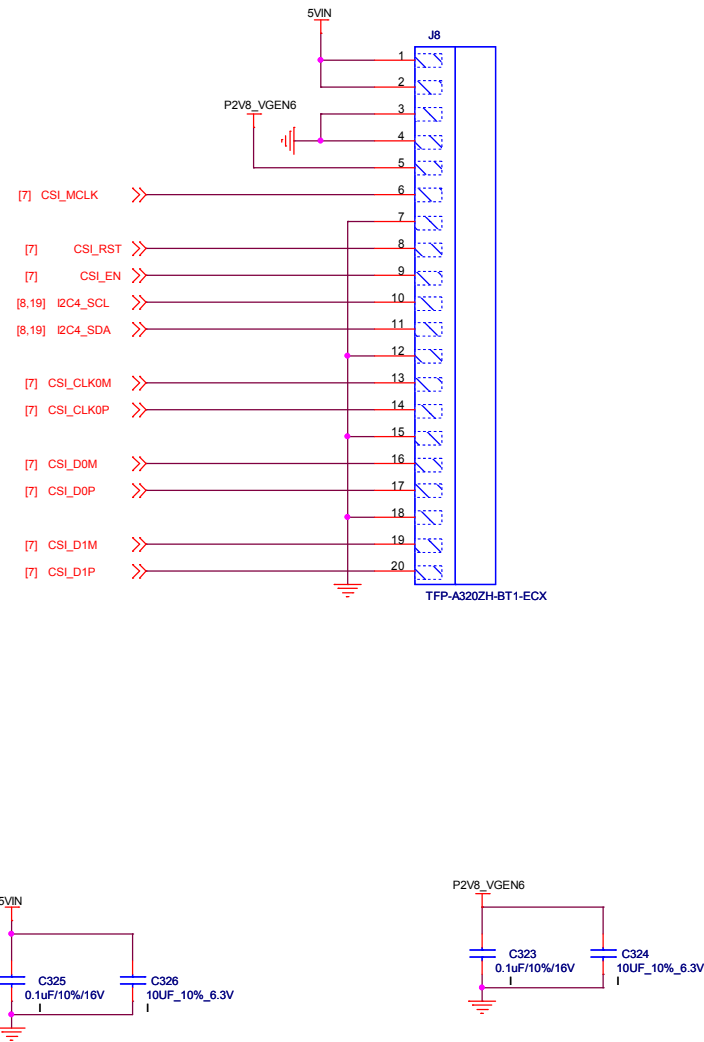


Design	XuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRiot Board		
Authorize	Qunsun	Size	Doc Name	Ver.
Standardize	<standardize>	A3	16 USB HUB	130701
		Date	Friday, December 13, 2013	Sheet 16 of 20

Parallel



CSI



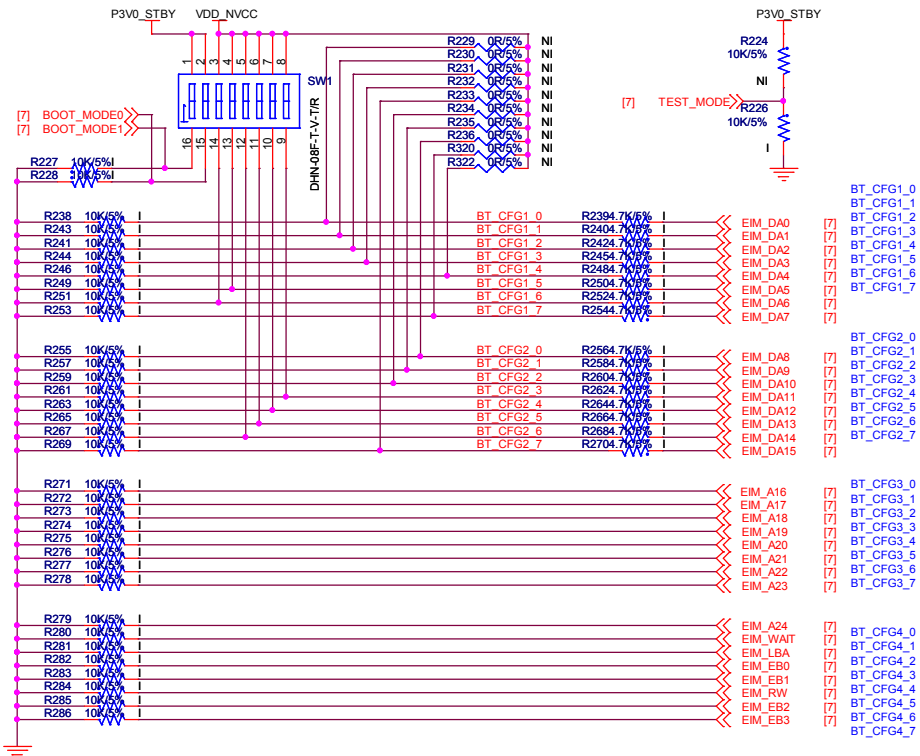
Design	XuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRlot Board		
Authorize	Qunsun	Size	Doc Name	Ver.
Standardize	<standardize>	A3	17 CAMERA	130701
		Date	Friday, December 13, 2013	Sheet 17 of 20

Table 7-1. Boot MODE Pin Settings

BOOT_MODE[1:0] ¹	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

1. BOOT_MODE[1:0] <- {BOOT_MODE1,BOOT_MODE0} (at rising edge of RESET_B)

BOOT DEV



NOTE:

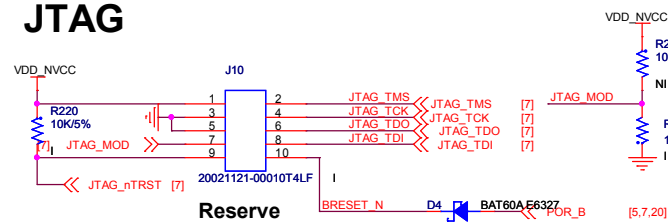
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilities include:

- 1) As close to processor as possible.
 - 2) Close to other componets using EIM signals.
- iMX solo don't support SATA feature

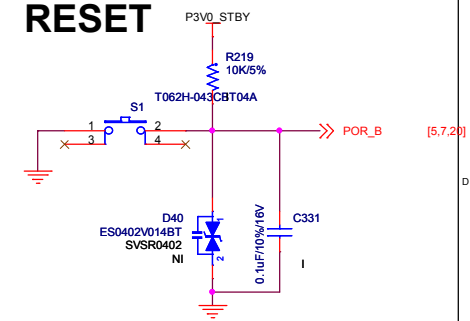
Boot Select Table

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 11 = SD4 Boot		01 = SD2 Boot 10 = SD3 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0

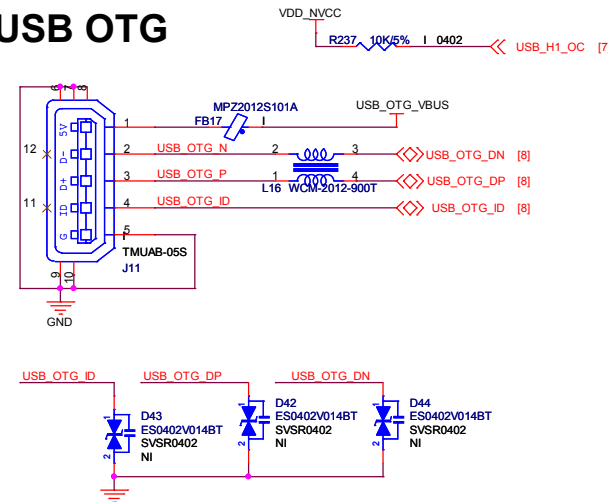
JTAG



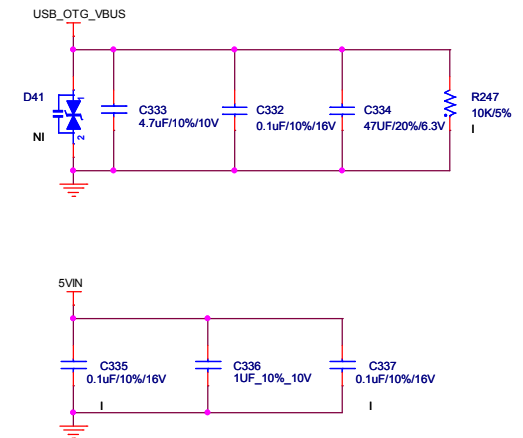
RESET



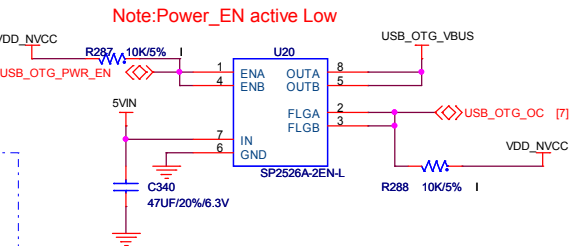
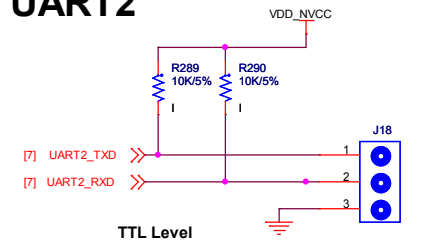
USB OTG



BOOT MODE



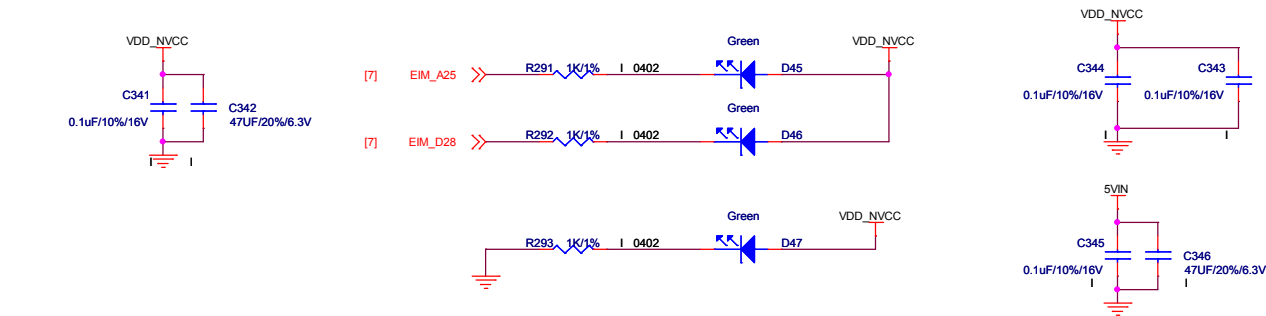
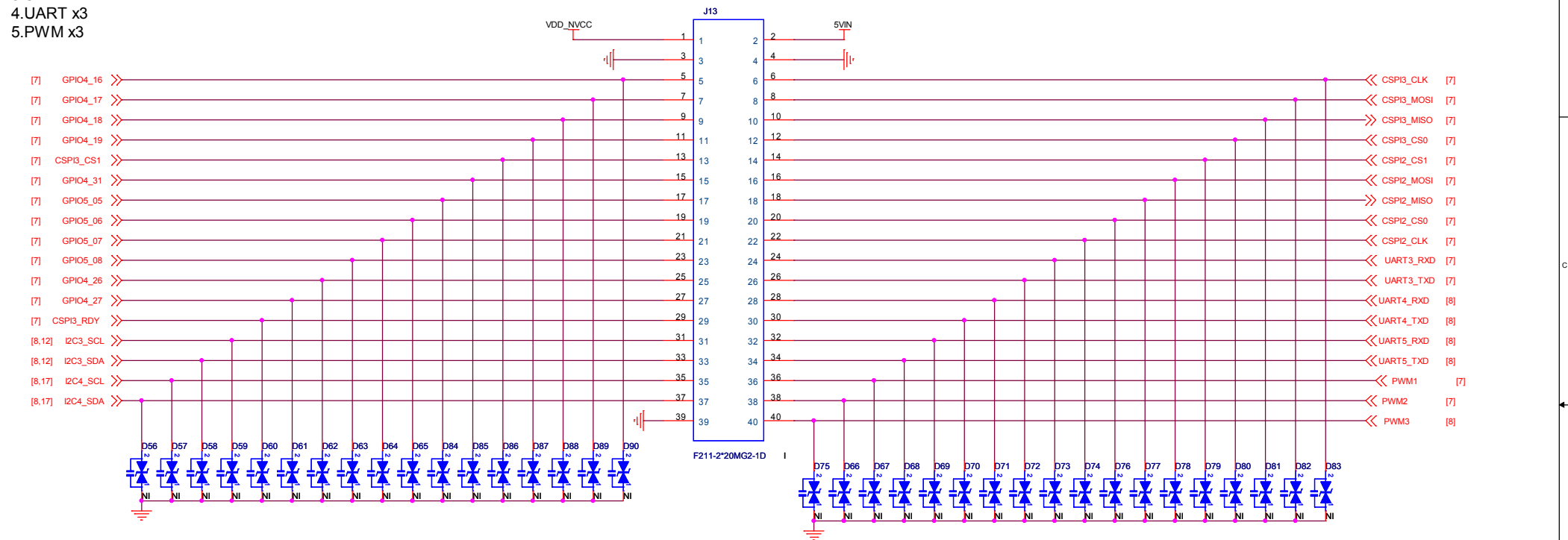
UART2



Design	xuZHH	Embest Technology Co.,Ltd.			
Review	ZHDP	TitleRiot Board			
Authorize	Qunsun	Size	Doc Name	Ver.	
Standardize	<standardize>	A3	18 BOOT/UART2	130701	
		Date	Friday, December 13, 2013	Sheet	18 of 20

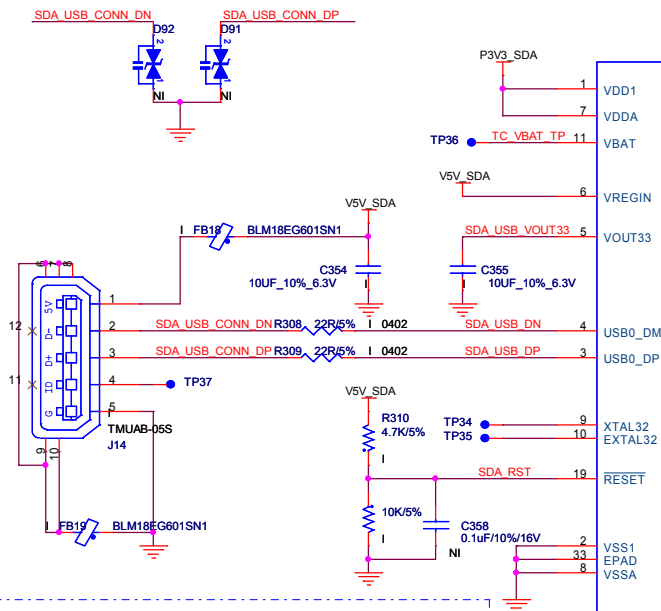
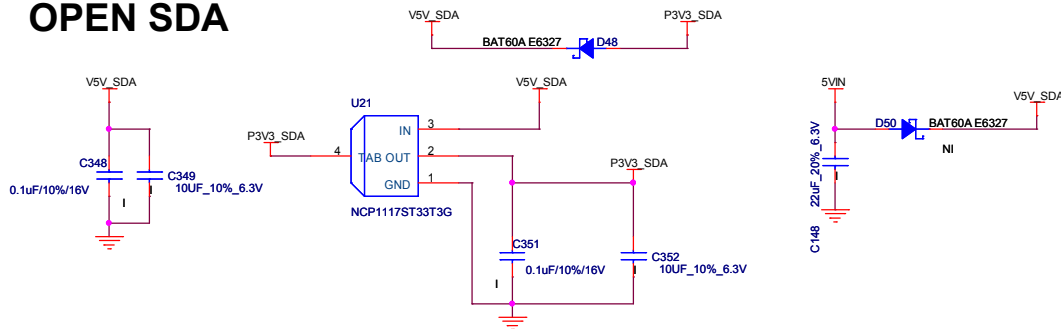
Expantion Port

- Expantion port include:
- 1.20bits RGB
 - 2.I2C x2
 - 3.SPI x2
 - 4.UART x3
 - 5.PWM x3

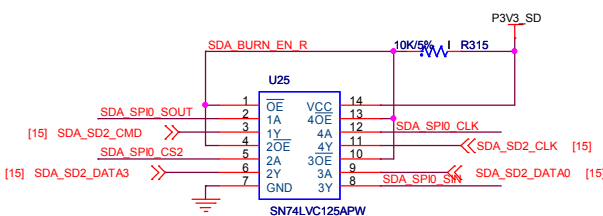


Design	xuZHH	Embest Technology Co.,Ltd.		
Review	ZHDP	TitleRlot Board		
Authorize	Qunsun	Size	Doc Name	Ver.
Standardize	<standardize>	A3	19 EXPANSION PORT	130701
		Date	Friday, December 13, 2013	Sheet 19 of 20

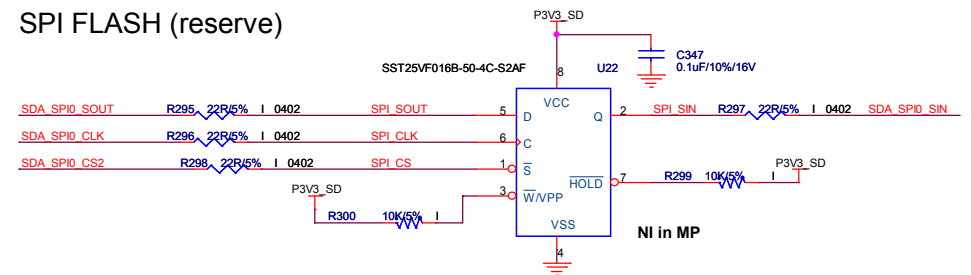
OPEN SDA



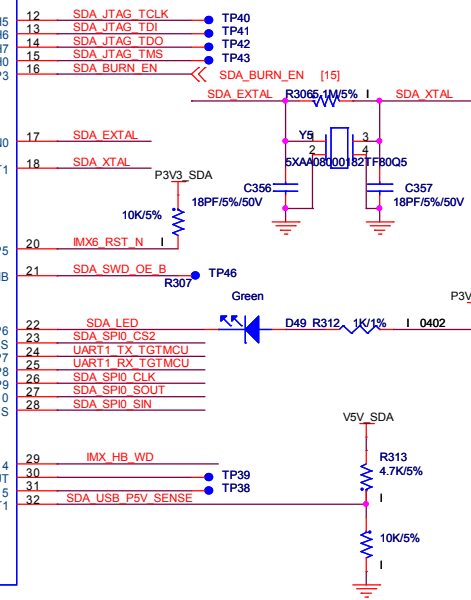
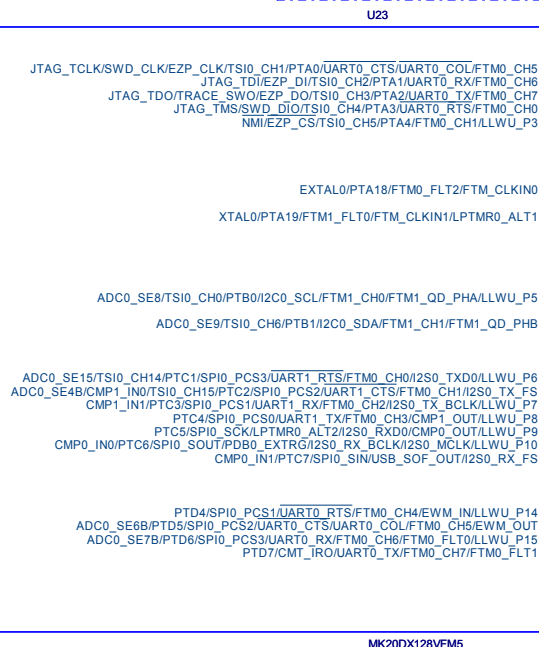
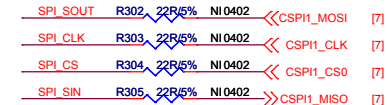
Pin #	SD Mode			SPI Mode		
	Name	Type ¹	Description	Name	Type ¹	Description
1	CD/DAT3 ²	I/O/PP ³	Card Detect/ Data Line [Bit 3]	CS	I ³	Chip Select (neg true)
2	CMD	I/O/PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1 ⁴	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2 ⁵	I/O/PP	Data Line [Bit 2]	RSV		



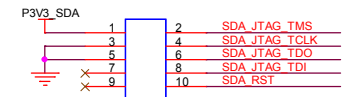
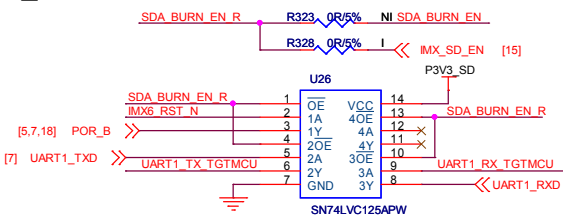
SPI FLASH (reserve)



Reserve for debug



SDA_MCU BUFFER



Design	XuZHH	Embest Technology Co.,Ltd.			
Review	ZHDP				
Authorize	Qunsun	TitleRlot Board			Ver. 130701
Standardize	<standardize>	Size A3	Doc Name 20 OPEN SDA		
		Date	Friday, December 13, 2013	Sheet	20 of 20