REV	Description	DATE	BY
V1.0	Initial production Release.	08/17 2015	Hugo
V1.1	A、Delete R455, R456 B、ADD U19 to make the VDD_RTC can be supply directly by a battery C、ADD R458~R476 and delete R422~R436 D、Off the connection of GPIO1_28 and GPIO2_0 to P8 E、Change the logic of Link_Light F、Delete U9, C35, U10, C36 to remove the USB protection. G、Fix the LCD data bit for 24bits display mode.	11/03 2015	Hugo

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Title: SOM-PH8700

Size: B | Document Number: P01_Title Page | Rev: Rev1.1

Draw By: Hugo | Date: Friday, April 01, 2016 | Sheet: 1 of 11

Design Guide

A、Because of the AM335x series CPU's display controler is specifical, the data bits fixs the color bits as the below shows:

3 Usage Notes and Known Design Exceptions to Functional Specifications

3.1 Usage Notes

This document contains Usage Notes. Usage Notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes may be incorporated into future documentation updates for the device (such as the device-specific data manual), and the behaviors they describe may or may not be altered in future device revisions.

3.1.1 LCD: Color Assignments of LCD_DATA Terminals

The blue and red color assignments to the LCD data pins are reversed when operating in RGB888 (24bpp) mode compared to RGB565 (16bpp) mode. In order to correctly display RGB888 data from the SGX, or any source formatted as RGB in memory, it is necessary to connect the LCD panel as shown in Figure 2. Using the LCD Controller with this connection scheme limits the use of RGB565 mode. Any data generated for the RGB565 mode requires the red and blue color data values be swapped in order to display the correct color.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIXEL_n																							
B[0]	G[0]	R[0]	B[1]	G[1]	R[1]	B[2]	R[2]	B[7:3]					G[7:2]						R[7:3]				

16-bit panel

24-bit panel

Figure 2. RGB888 Mode LCD Controller Output Pin Mapping (LCD_DATA[23:0])

When operating the LCD Controller in RGB565 mode the LCD panel should be connected as shown in Figure 3. Using the LCD Controller with this connection scheme limits the use of RGB888 mode. Any data generated for the RGB888 mode requires the red and blue color data values be swapped in order to display the correct color.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIXEL_n																							
0	0	0	0	0	0	0	0	R[7:3]					G[7:2]						B[7:3]				

16-bit panel

B、In this design, the display controler is used for 24bit display mode, as page P11_Connector shows, it is not fixed one by one to LCD_DATA* sternly.

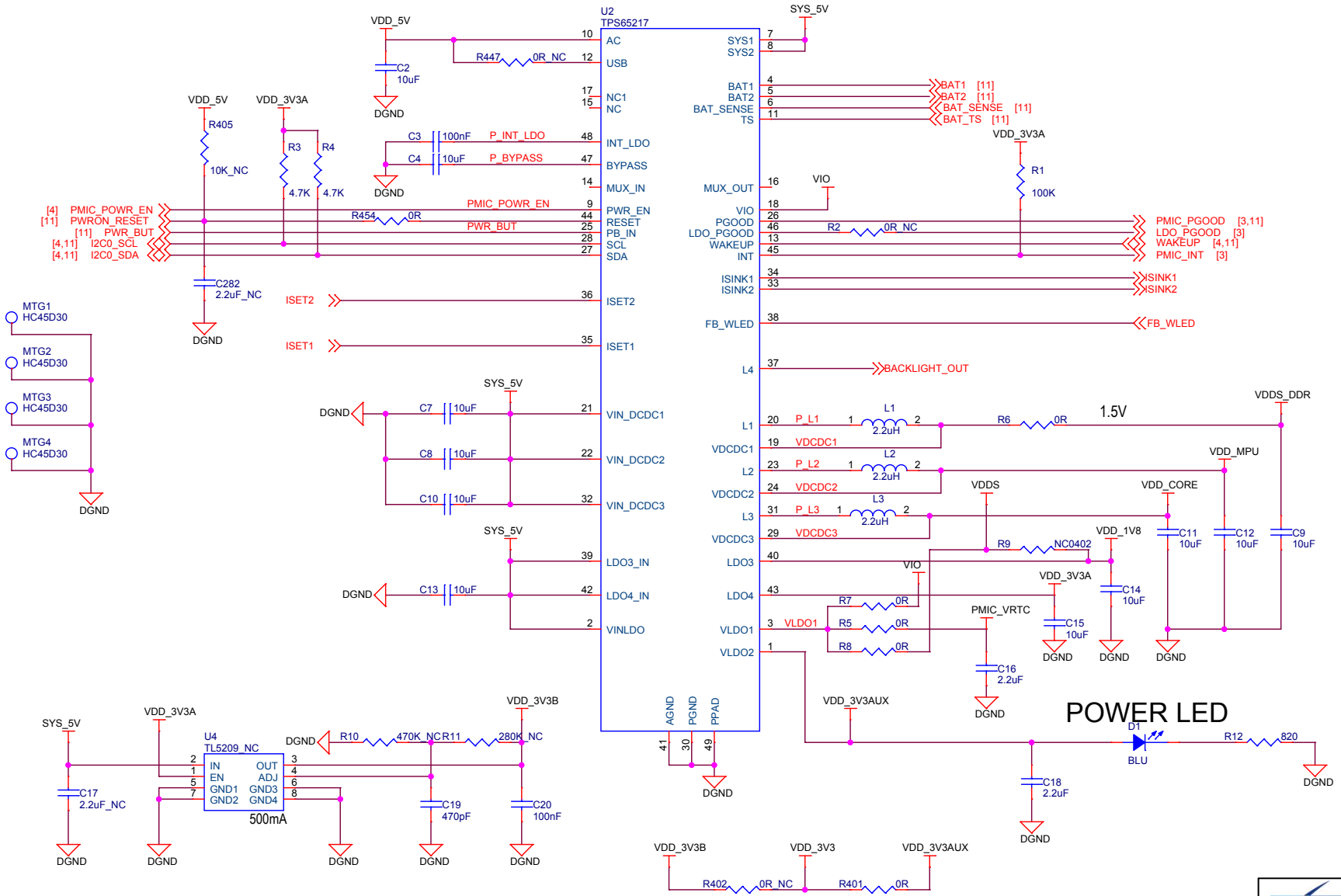
C、If it is design for 16bits display mode, the designer should use the follow matchup for their design:

P1.52(LCD_DATA0) for BLUE3, P1.54(LCD_DATA1) for BLUE4, P1.56(LCD_DATA2) for BLUE5, P1.58(LCD_DATA3) for BLUE6, P1.60(LCD_DATA4) for BLUE7
P1.55(LCD_DATA5) For GREEN2, P1.32(LCD_DATA6) For GREEN3, P1.34(LCD_DATA7) For GREEN4, P1.36(LCD_DATA8) For GREEN5, P1.38(LCD_DATA9) For GREEN6, P1.40(LCD_DATA10) For GREEN7
P1.41(LCD_DATA11) For RED3, P1.43(LCD_DATA12) For RED4, P1.45(LCD_DATA13) For RED5, P1.47(LCD_DATA14) For RED6, P1.49(LCD_DATA15) For RED7

P1.35(LCD_DATA23), P1.51(LCD_DATA22), P1.46(LCD_DATA21), P1.37(LCD_DATA20), P1.53(LCD_DATA19), P1.48(LCD_DATA18), P1.39(LCD_DATA17), P1.50(LCD_DATA16) can be used for other Pinmux

D、The I2C bus has been used a 4.7k resistor pull up on the module

Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCod
Date: Friday, April 01, 2016		Sheet 1 of 1	



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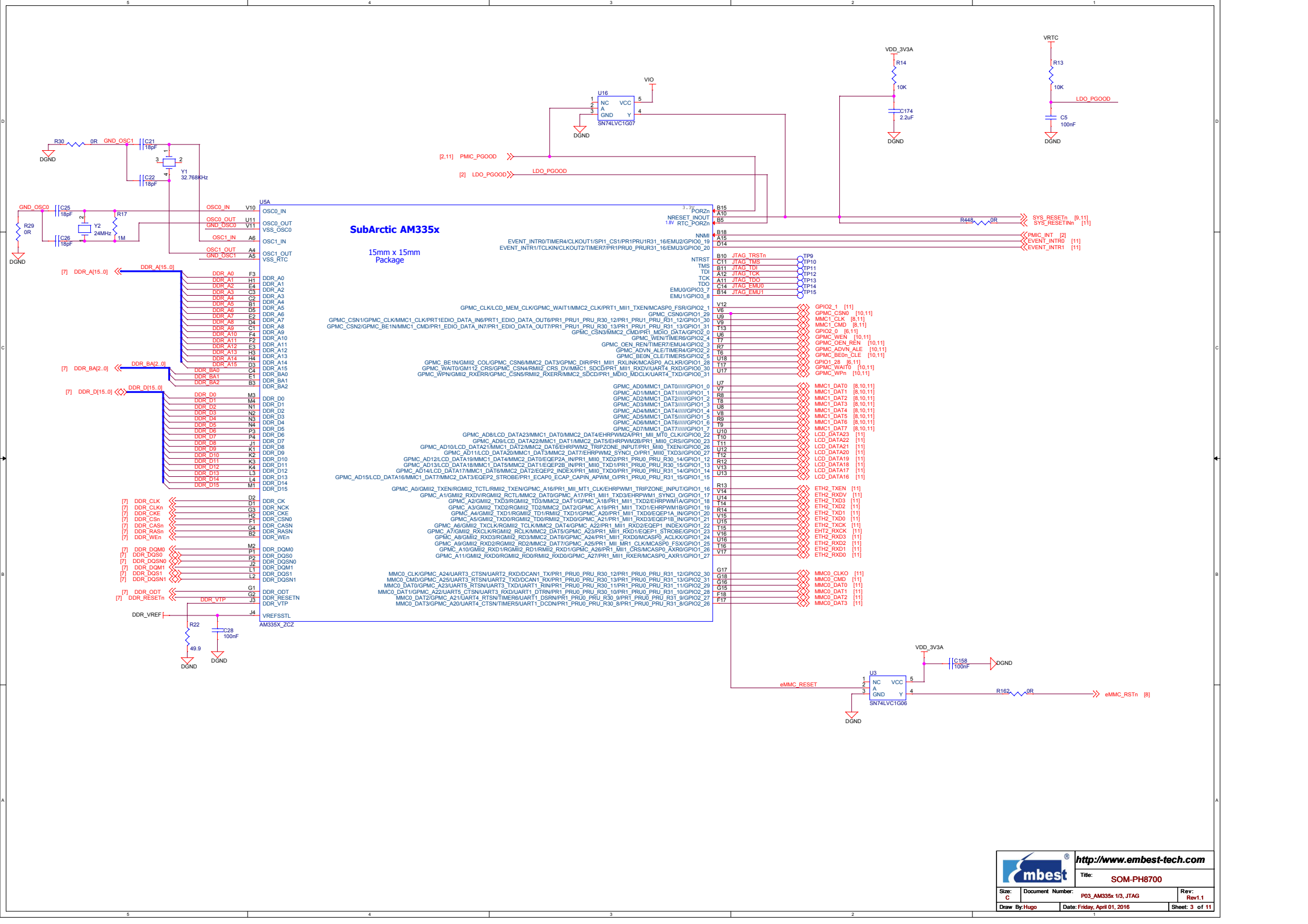
Size: B	Document Number: P02_Power Management	Rev: Rev1.1
Draw By: Hugo	Date: Friday, April 01, 2016	Sheet: 2 of 11



http://www.embest-tech.com			
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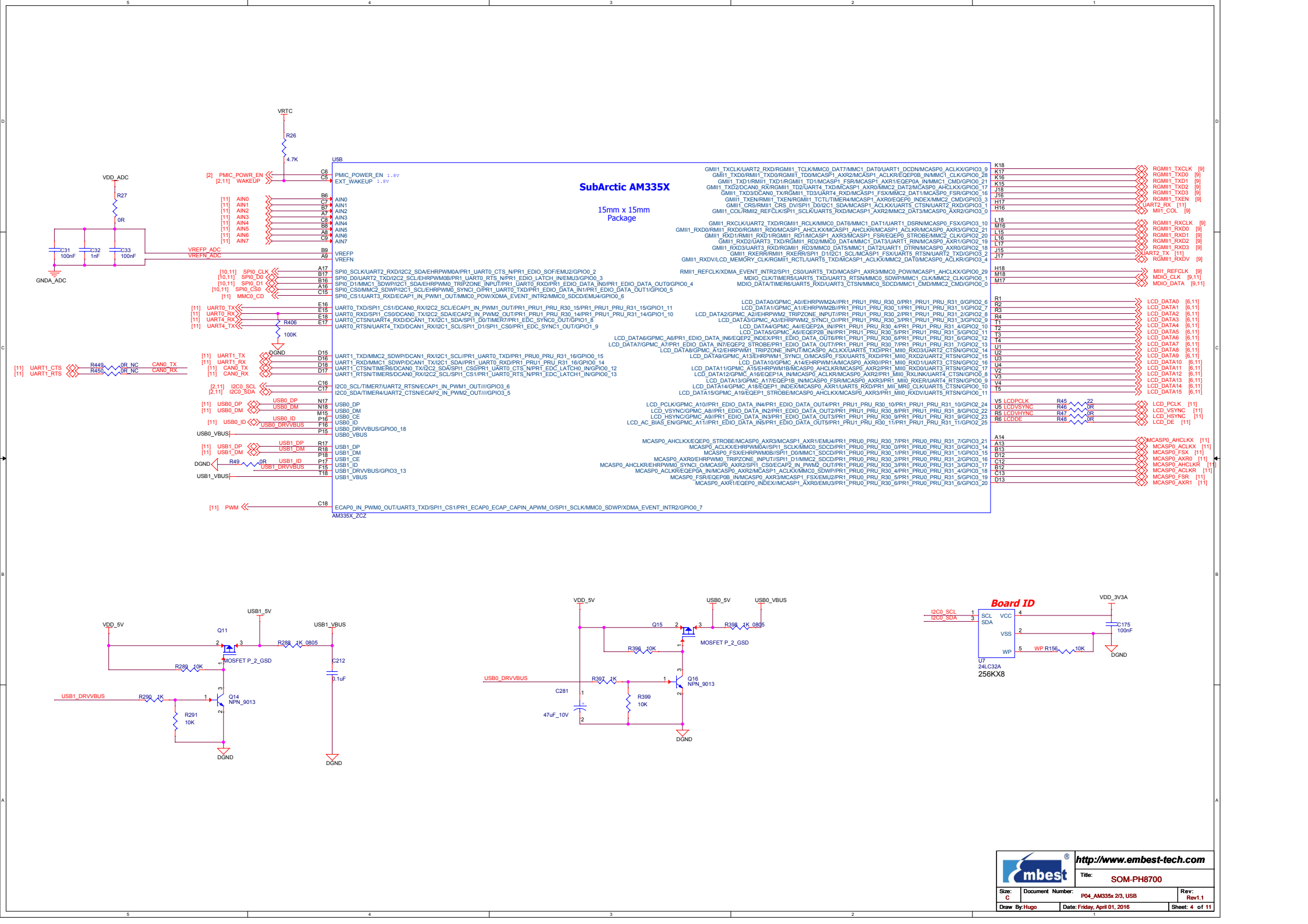
Draw By: Hugo	Date: Friday, April 01, 2016		Sheet: 3 of 11



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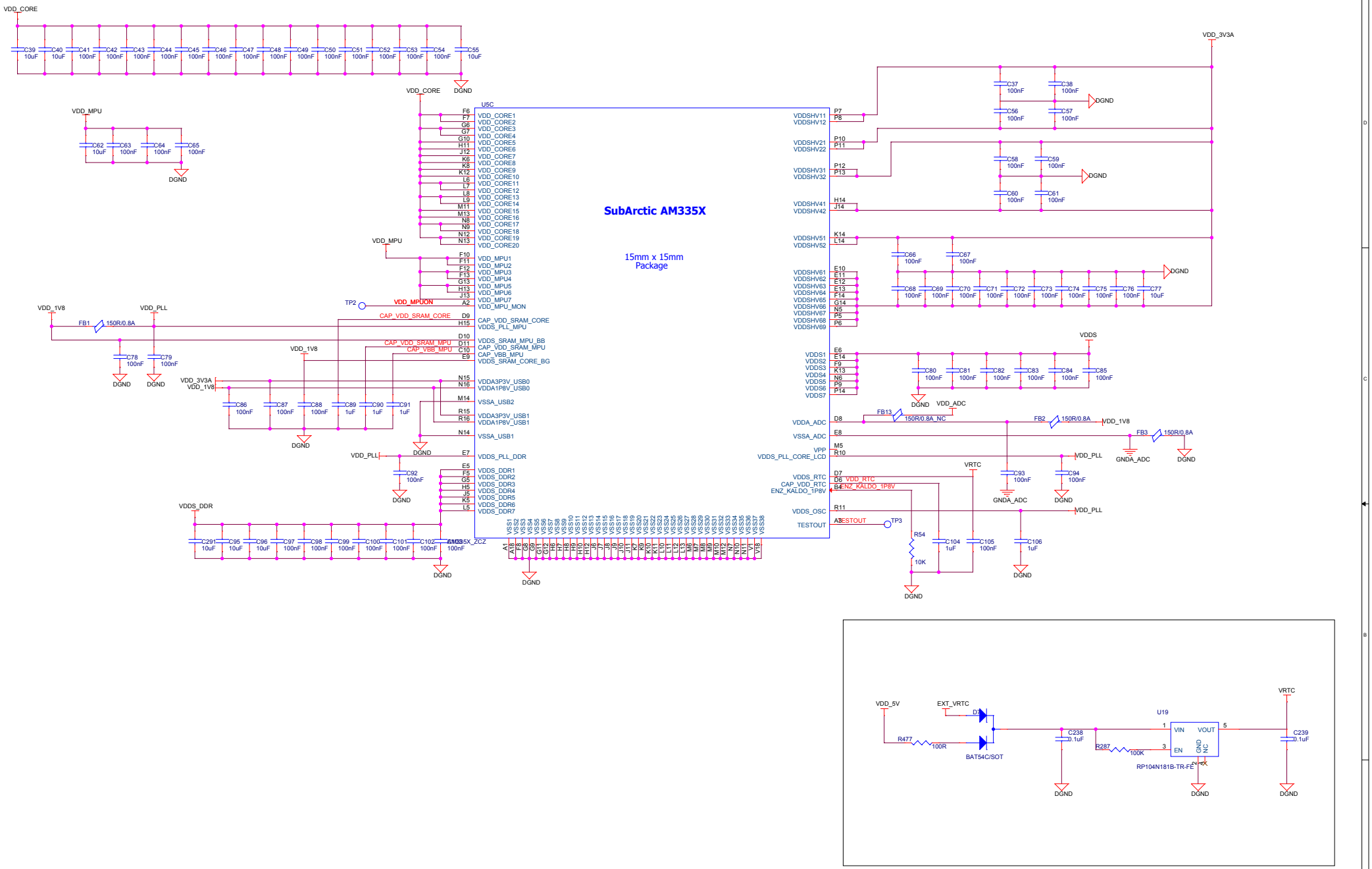
Size: C	Document Number: P04_AM335x 2/3, USB	Rev: Rev1.1	
Draw By: Hugo	Date: Friday, April 01, 2016	Sheet: 4 of 11	



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Size: C	Document Number: P05_AM335x 3/3	Rev: Rev1.1	
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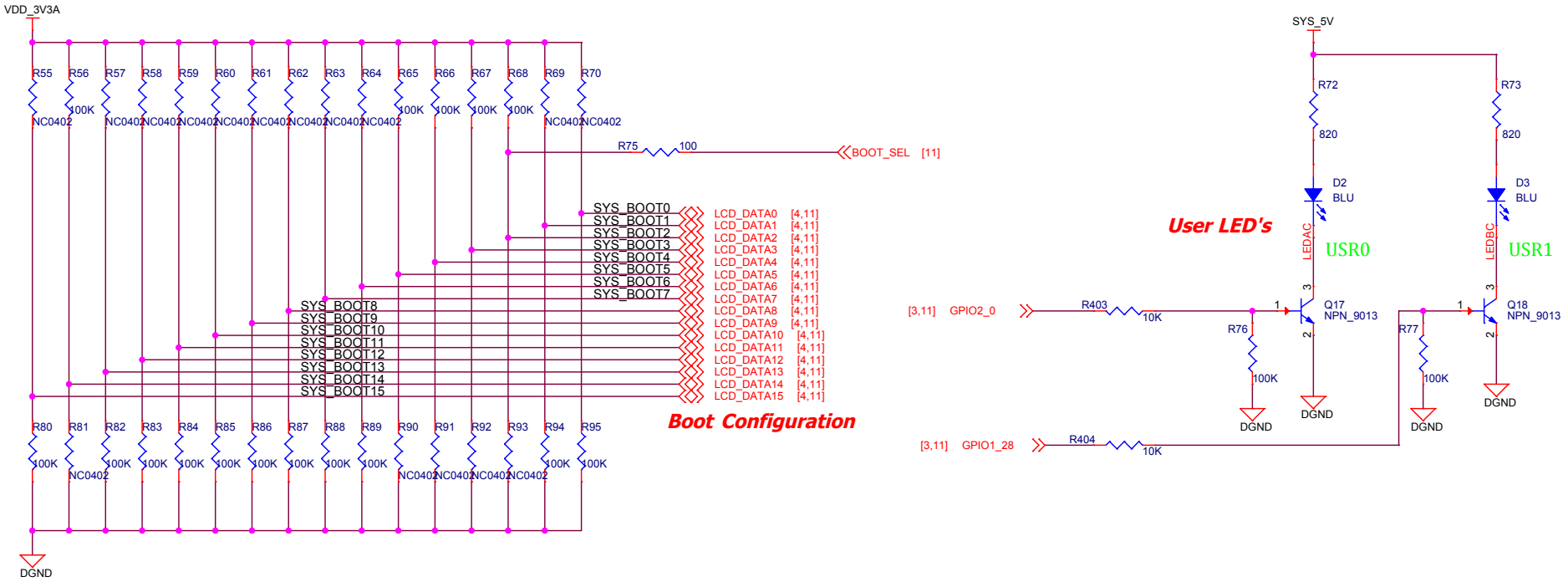

SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5]	UART0

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Title: SOM-PH8700			
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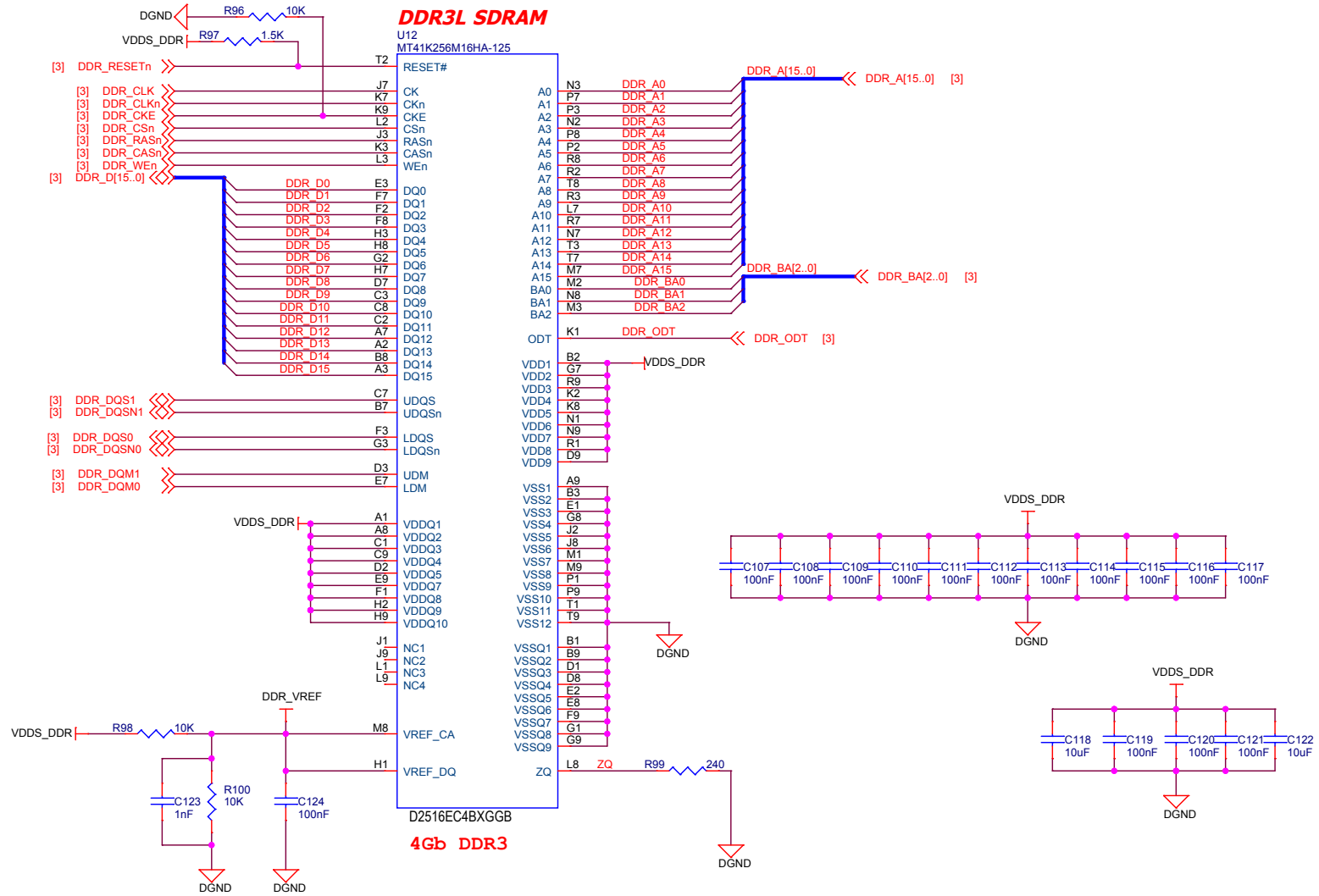

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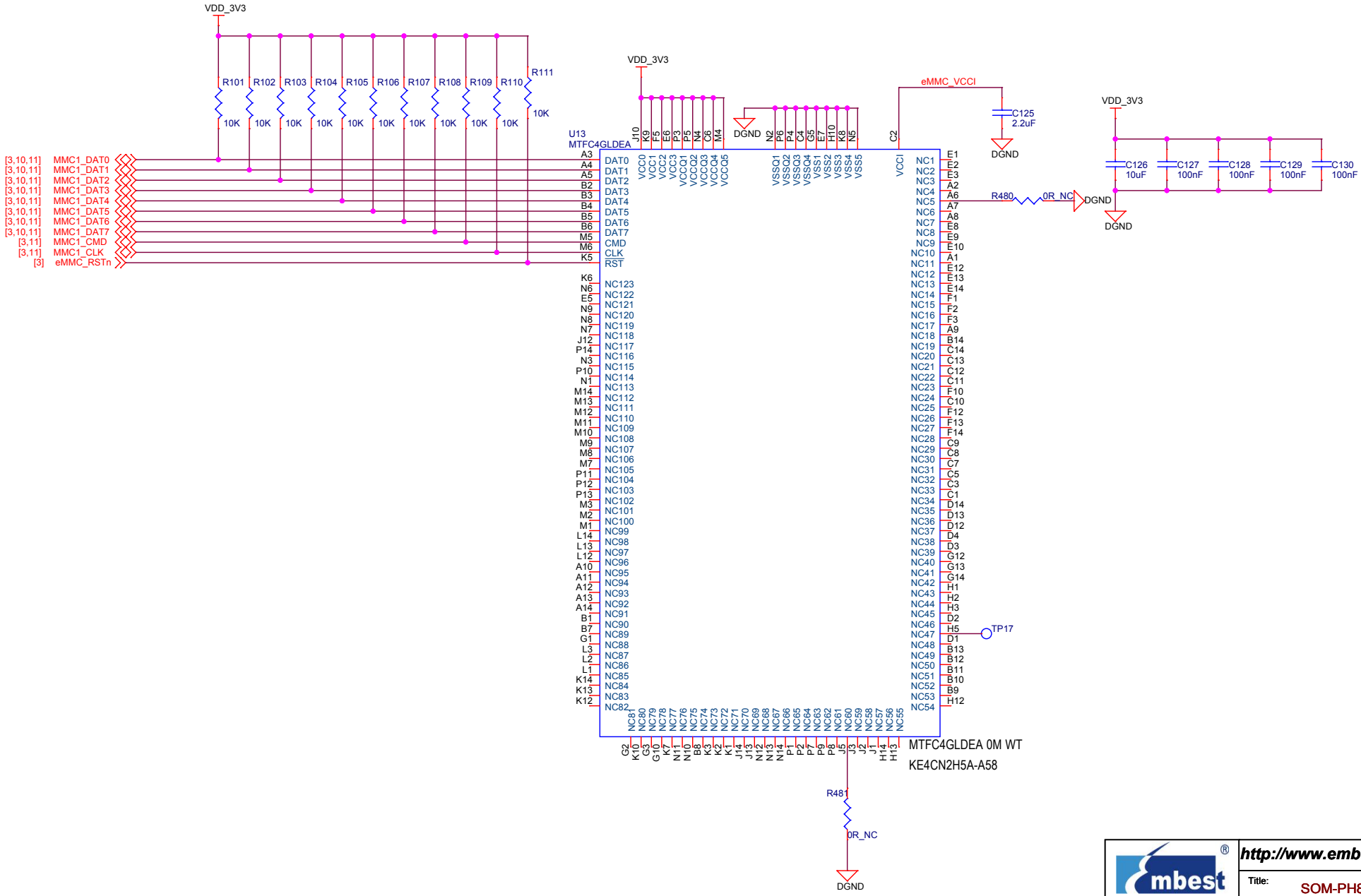
Title: SOM-PH8700		
Size: B	Document Number: P07_DDR3 Memory	Rev: Rev1.1
Draw By: Hugo	Date: Friday, April 01, 2016	Sheet: 7 of 11



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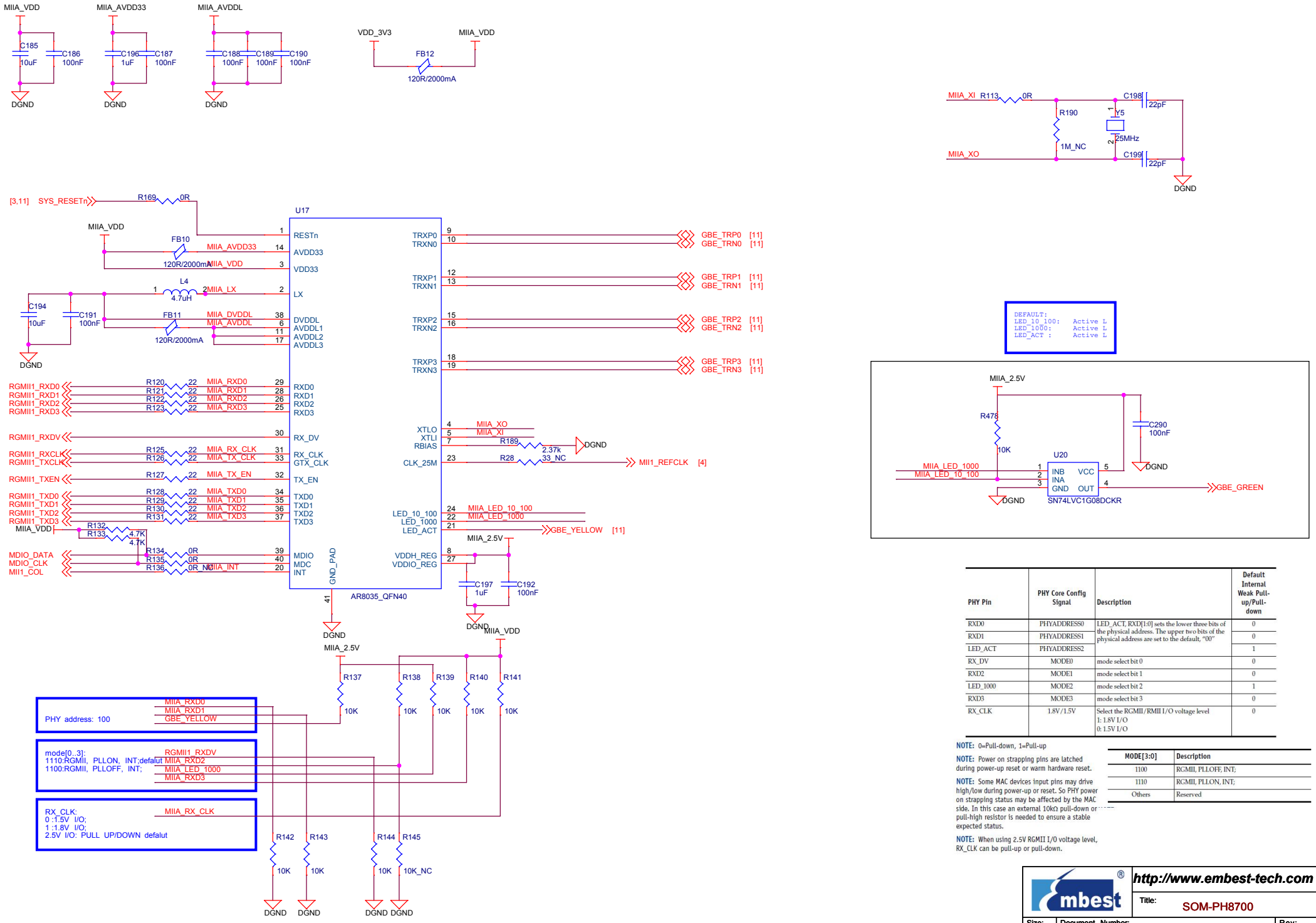
Title: SOM-PH8700		
Size: B	Document Number: P08_eMMC FLASH	Rev: Rev1.1
Draw By: Hugo	Date: Friday, April 01, 2016	Sheet: 8 of 11



PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/Pull-down
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE0	mode select bit 0	0
RXD2	MODE1	mode select bit 1	0
LED_1000	MODE2	mode select bit 2	1
RXD3	MODE3	mode select bit 3	0
RX_CLK	1.8V/1.5V	Select the RGMII/RMII I/O voltage level 1: 1.8V I/O 0: 1.5V I/O	0

NOTE: 0=Pull-down, 1=Pull-up

NOTE: Power on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10kΩ pull-down or pull-high resistor is needed to ensure a stable expected status.

NOTE: When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

MODE[3:0]	Description
1100	RGMII, PLLOFF, INT;
1110	RGMII, PLLON, INT;
Others	Reserved

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Title: SOM-PH8700		
Size: A3	Document Number: P09_10/100/1000 Ethernet	Rev: Rev1.1
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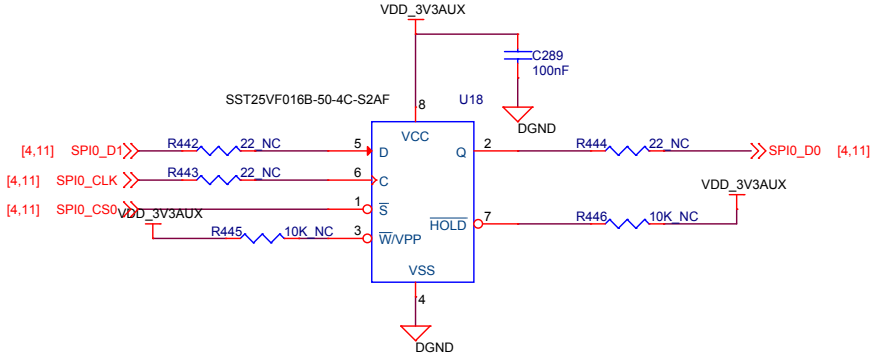
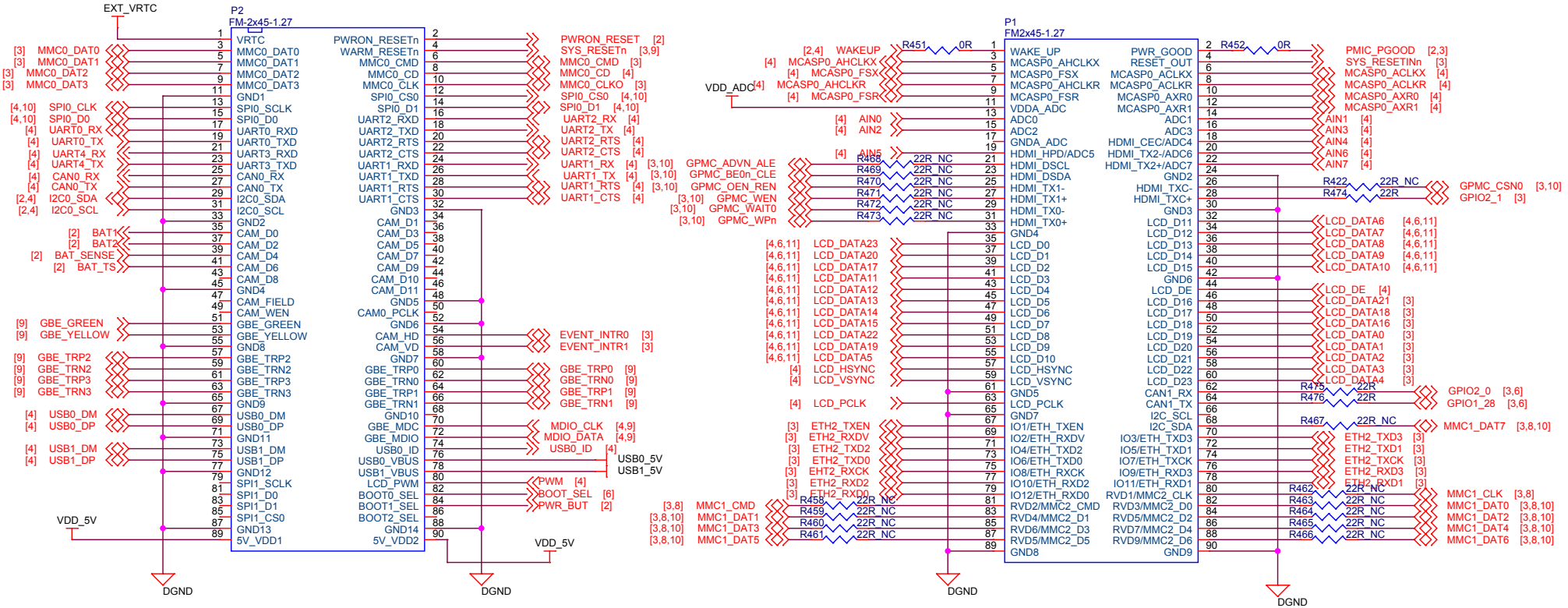


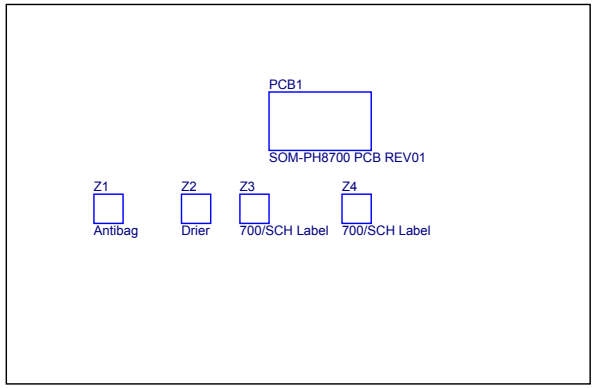
26.1.7.6.4 *Pins Used*

The list of device pins that are configured by the ROM incase of SPI boot mode are as follows. Please note that all the pins might not be driven at boot time.

Table 26-28. Pins Used for SPI Boot

Signal name	Pin Used in Device
cs	spi0_cs0
miso	spi0_d0
mosi	spi0_d1
clk	spi0_sclk





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