PAGE NO.	SCHEMATIC PAGE
1	01 Cover Page
2	02 System Block
3	03 Power System Block
4	04 PMIC1
5	05 PMIC2
6	06 CPU Power
7	07 IMX6Q_SOC_A
8	08 IMX6Q_SOC_B
9	09 IMX6Q_SOC_C
10	10 DDR3
11	11 eMMC
12	12 Boot Select
13	13 GBE
14	14 EEPROM & JTAG
15	15 SMARC Connector
16	16 Design History

Design	<design>		
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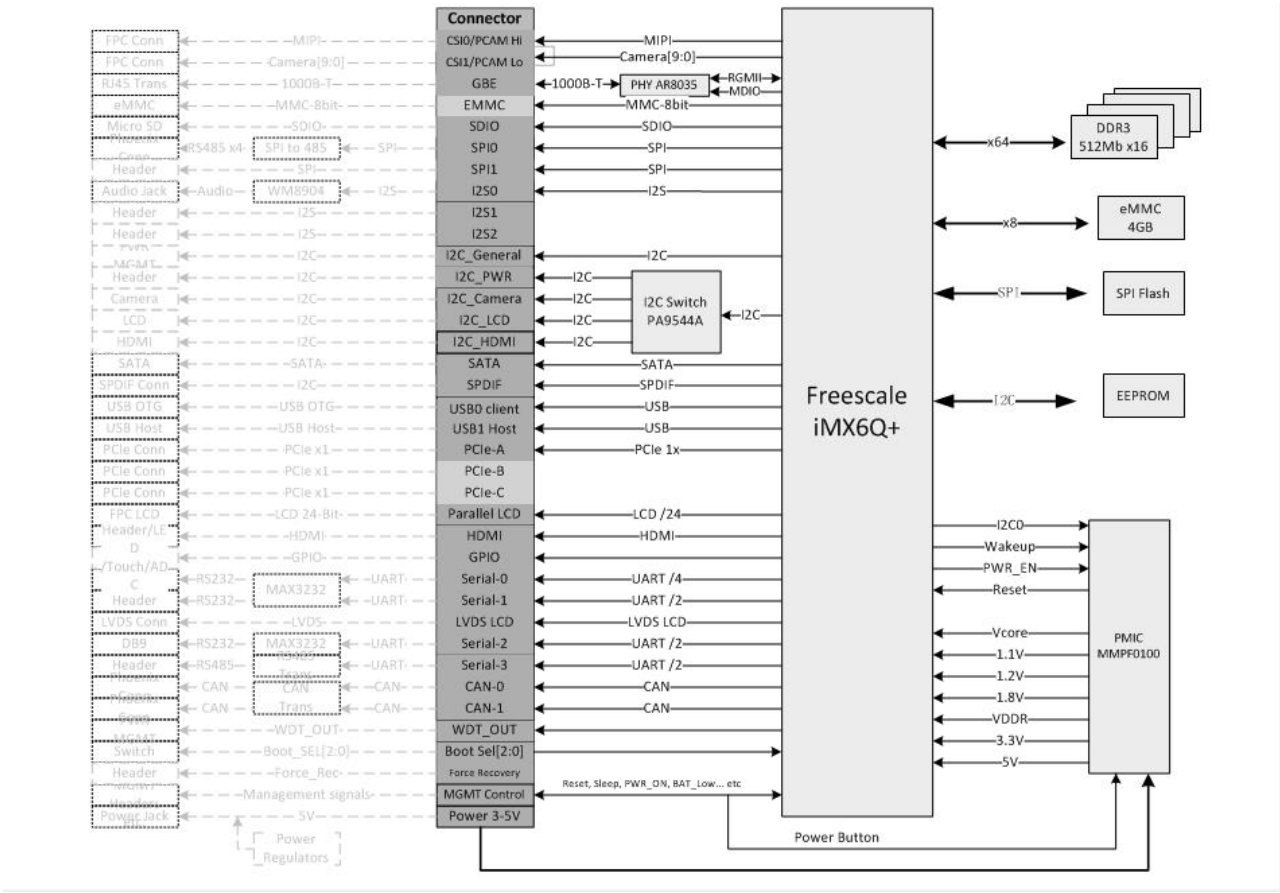
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6 / Ver. V0.0
Standardize	<standardize>	Date Friday, March 08, 2019	Sheet 1 of 16



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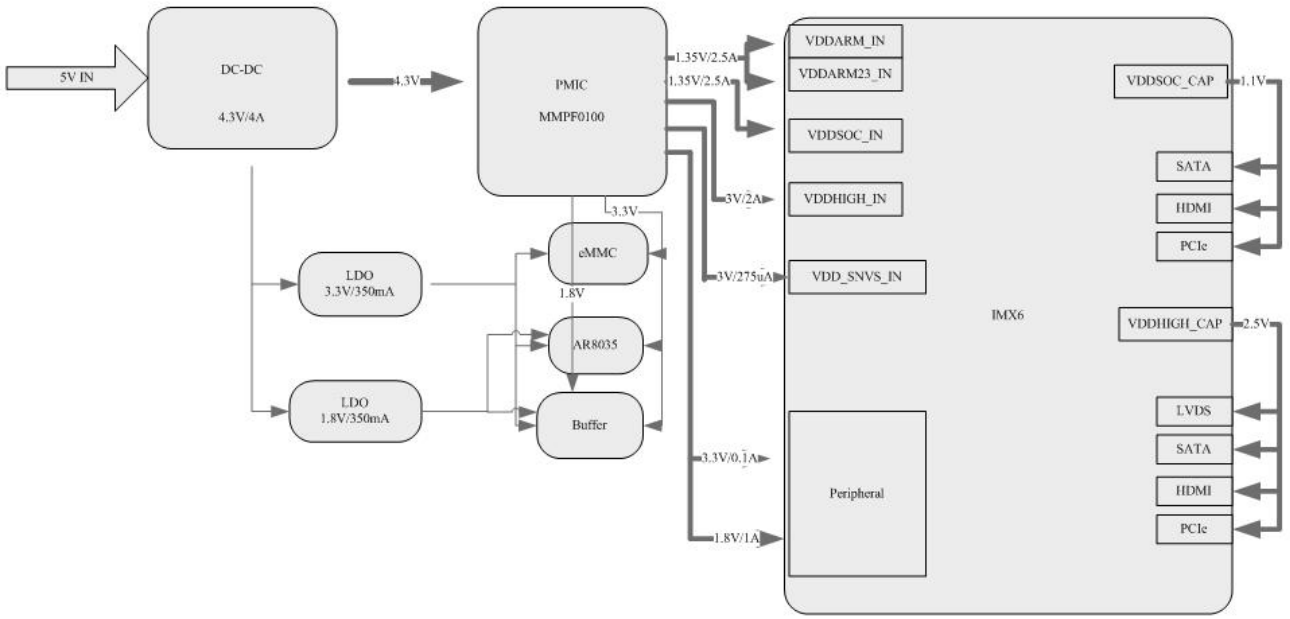
Standardize	<standardize>	Date Friday, March 08, 2019	Sheet 2 of 16



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Review	<review>	Title 03 Power System Block	
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6 Ver. V0.0
Standardize	<standardize>	Date Friday, March 08, 2019	Sheet 3 of 16

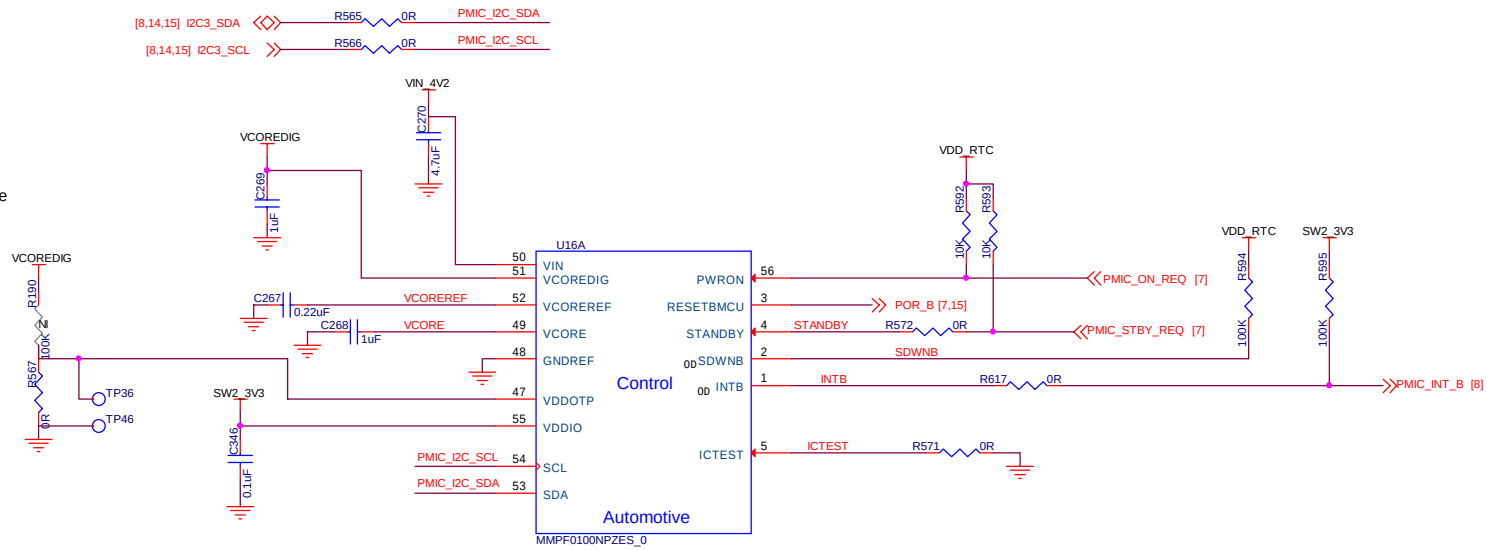
VCOREDIG(Digital Core supply) is a 1.5V output voltage, when PF0100 into the Off mode,Only VCOREDIG and VSNVS are powered in the mode of operation

VCOREREF:Main band gap reference
All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF

The PF0100 can be configured to start-up from either the internal OTP configuration, or with a hard-coded configuration built in to the device. The internal hard-coded configuration is enabled by connecting the VDDOTP pin to VCOREDIG through a 100 kohm resistor. The OTP configuration is enabled by connecting VDDOTP to GND.

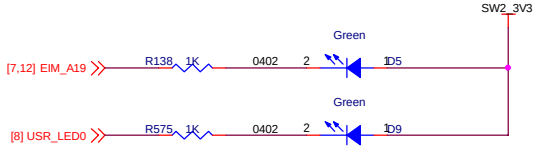
VCORE: Output. Analog Core supply

VDDOTP Programming Mode External Power - Remove pull-up resistor, and connect test point to 8 volts to program PMIC fuses, bypassed with 10 to 20pF of capacitance, install series resistor after programming the efuse.



	VSNVS	SW1AB	SW1C	SW2	SW3A	SW3B	SW4	SWBST	VREFDDR	VGEN1	VGEN2	VGEN3	VGEN4	VGEN5	VGEN6
Maximum Load Curren	0.4mA	2500mA	2000mA	2500mA	1250mA		1000mA	600mA	10mA	100mA	250mA	100mA	350mA	100mA	200mA
Default	3.0V	1.375V	1.375V	3.0V	1.5V	1.5V	1.8V	-	0.75V	-	1.5V	-	1.8V	2.5V	2.8V
F0 OTP	3.0V	1.375V	1.375V	3.3V	1.5V		3.15V	5V	-	1.5V	1.5V	2.5V	1.8V	2.8V	3.3V

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN VDD_ARM23_IN[3]	1.35[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.225 V minimum for operation up to 852 MHz or 996 MHz (depending on the device speed grade).
		1.275[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.150 V minimum for operation up to 792 MHz.
		1.05[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 0.925 V minimum for operation up to 396 MHz.
	VDD_SOC_IN[6]	1.350[4]	—	1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum.
		1.275[4,7]	—	1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.

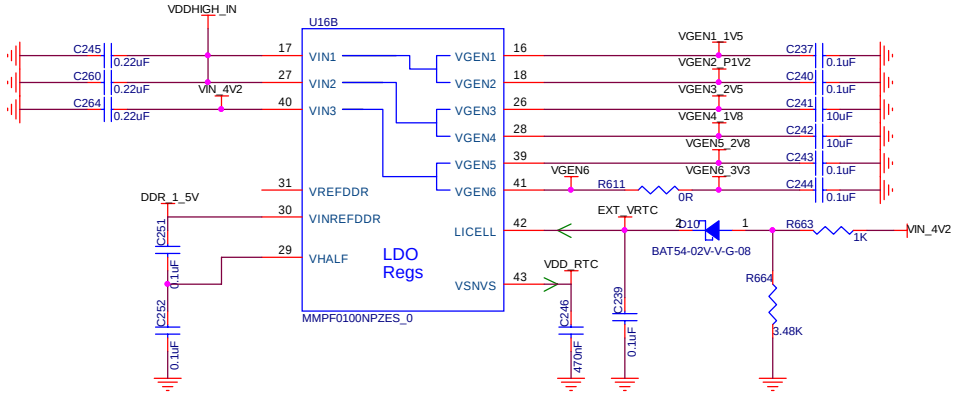


PCB1 PCB

Design	<design>	Title	04 PMIC1
Review	<review>		
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6 Ver. V0.0
Standardize	<standardize>	Date	Sunday, July 21, 2019 Sheet 4 of 16

PMIC

With low-inductive paths between VIN the voltage sources, either 0.22 uF or 0.47 uF may be used.



NVCC_RGMII is supply by AR8035, but set VGEN1 to output 1.8V for debug

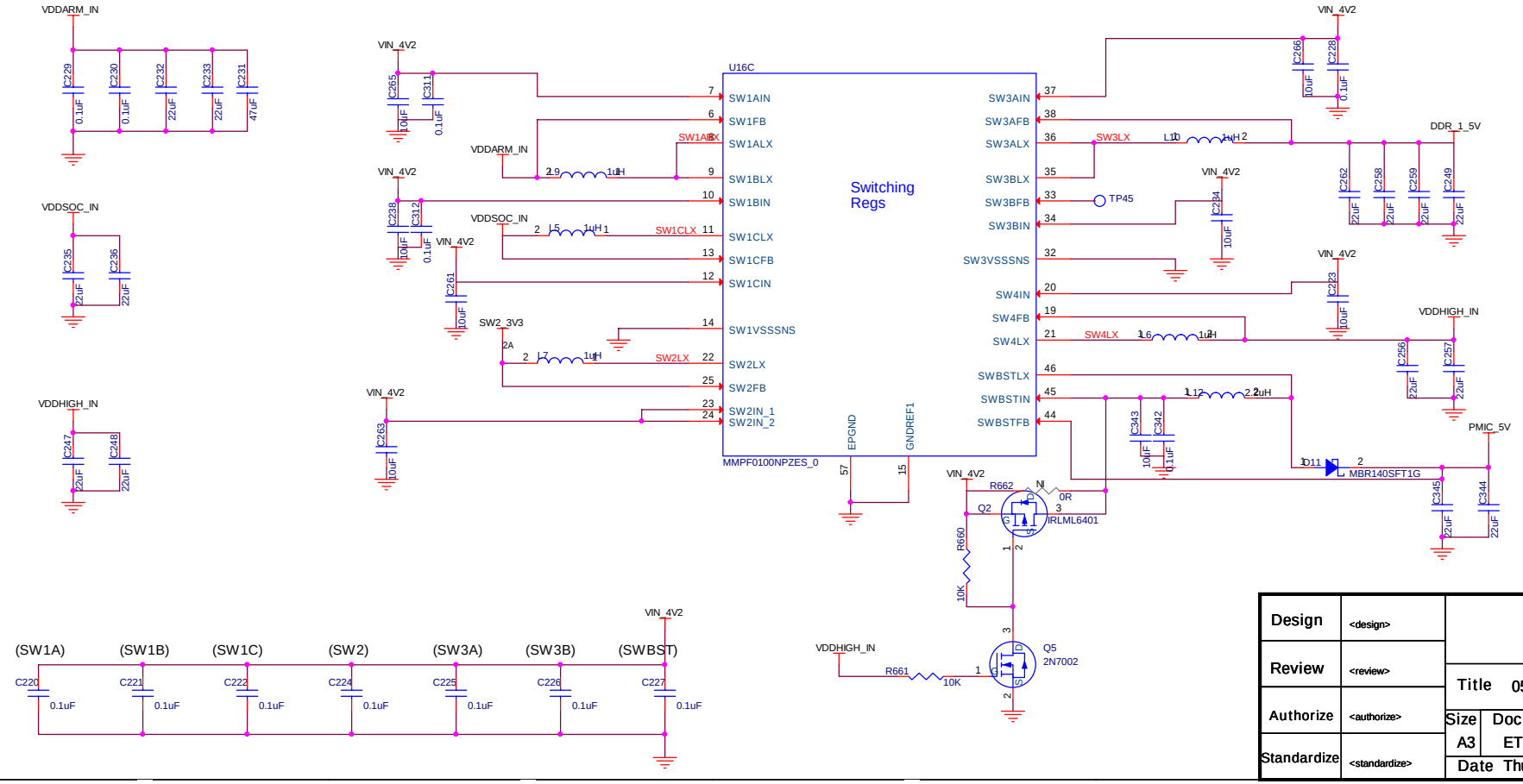
NVCC_PLL_OUT is not a power supply for iMX6, but set VGEN2 to output 1.2V for debug

VGEN3_2V5 output 2.5V for sata debug

VGEN4 output 2.5V for I2C switch power supply

VGEN5_3V3 output 3.3V for NVCC_SD2

VSNVS is supplied by either the main input supply or the coin cell



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Review	<review>		
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6 Ver. V0.0
Standardize	<standardize>	Date	Thursday, March 21, 2019 Sheet 5 of 16

U1E
MCIMX6Q7CVT08AC

i.MX6Q - POWER

VDDARM_IN
VDDARM23_IN
VDDSOC_IN
for all,
max:1.35V/2.37A
VDDHIGH_IN
VDD_RTC
VDD_SNVS_IN
275uA

FB2
MPZ2012S101A

D3
BAT60A E6327

iMX6S	
iMX6DL	
iMX6D	
iMX6Q	

MH2 NI
MH1 NI
mhc40d20 mhc40d20

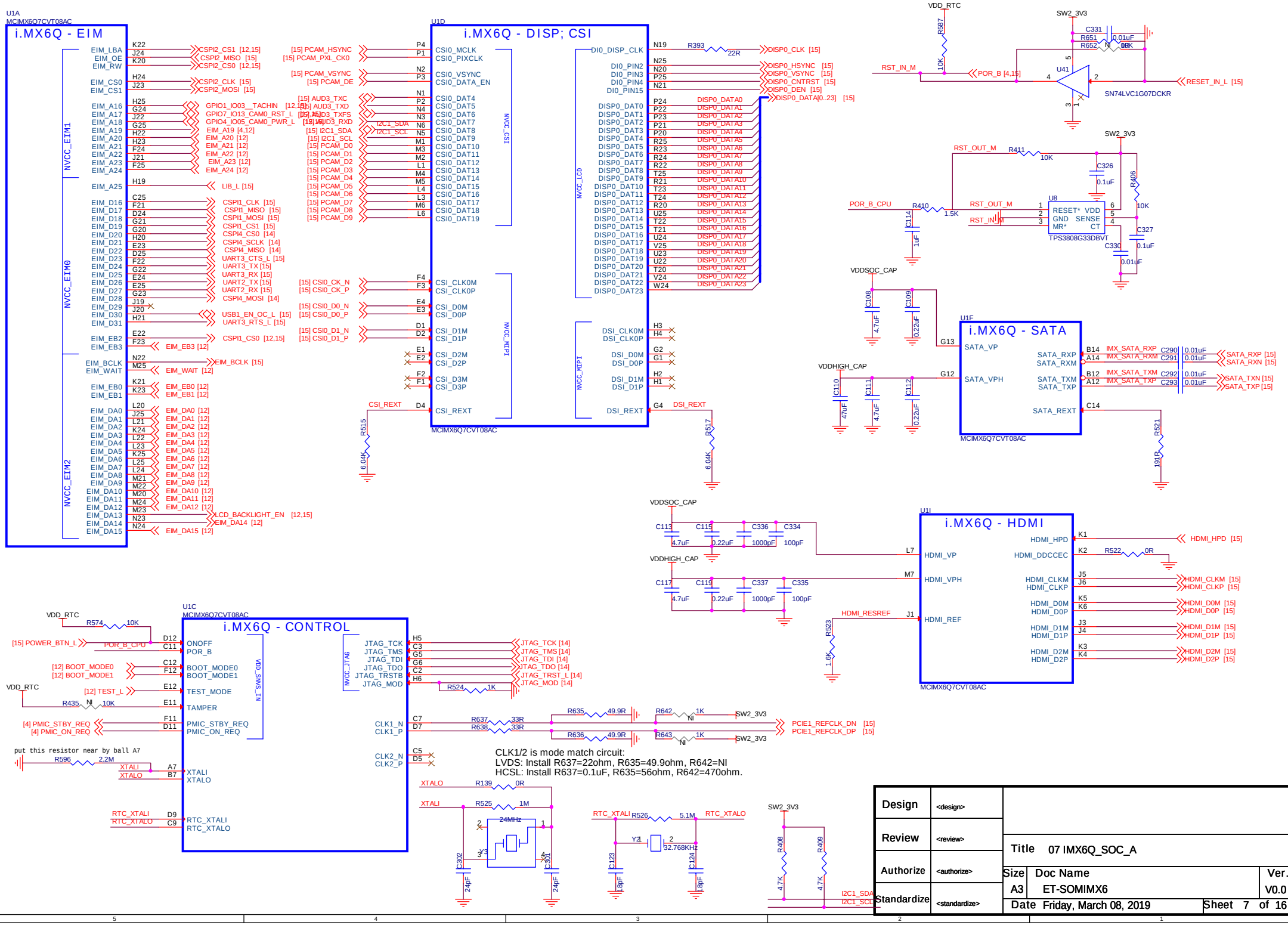
VDDARM_CAP
VCCARM23_CAP
VDDSOC_CAP
VDDPU_CAP
VDDHIGH_CAP
VDD_SNVS_CAP
VGEN2_P1V2
VGEN3_2V5
NVCC_PLL_OUT
SW2_3V3

Do not connect any loads to VDDARM_CAP, VDDARM23_CAP, or VDDPU_CAP

Install for Quad and not install for Dual, for dual,one of the cap instead of a 0R res

TP48

Design	<design>	
Review	<review>	Title 06 CPU Power
Authorize	<authorize>	Size A3 Doc Name ET-SOMIMX6 Ver. V0.0
Standardize	<standardize>	Date Monday, March 11, 2019 Sheet 6 of 16


U1A
MCIMX6Q7CVT08AC
i.MX6Q - EIM
NVCC_EIM1
NVCC_EIM0
NVCC_EIM2
EIM_LBA K22
EIM_OE J24
EIM_RW K20
EIM_CS0 H24
EIM_CS1 J23
EIM_A16 H25
EIM_A17 G24
EIM_A18 J22
EIM_A19 G25
EIM_A20 H22
EIM_A21 H23
EIM_A22 F24
EIM_A23 J21
EIM_A24 F25
EIM_A25 H19
EIM_D16 C25
EIM_D17 F21
EIM_D18 D24
EIM_D19 G21
EIM_D20 G20
EIM_D21 H20
EIM_D22 E23
EIM_D23 D25
EIM_D24 F22
EIM_D25 G22
EIM_D26 E24
EIM_D27 E25
EIM_D28 G23
EIM_D29 J19
EIM_D30 J20
EIM_D31 H21
EIM_EB2 E22
EIM_EB3 F23
EIM_BCLK N22
EIM_WAIT M25
EIM_EB0 K21
EIM_EB1 K23
EIM_DA0 L20
EIM_DA1 J25
EIM_DA2 L21
EIM_DA3 K24
EIM_DA4 L22
EIM_DA5 L23
EIM_DA6 K25
EIM_DA7 L25
EIM_DA8 L24
EIM_DA9 M21
EIM_DA10 M22
EIM_DA11 M20
EIM_DA12 M24
EIM_DA13 M23
EIM_DA14 N23
EIM_DA15 N24
CSPI2_CS1 [12,15]
CSPI2_MISO [15]
CSPI2_CS0 [12,15]
CSPI2_CLK [15]
CSPI2_MOSI [15]
GPIO1_IO03__TACHIN [12,15]
GPIO7_IO13_CAM0_RST_L [12,15]
GPIO4_IO05_CAM0_PWR_L [12,15]
EIM_A19 [4,12]
EIM_A20 [12]
EIM_A21 [12]
EIM_A22 [12]
EIM_A23 [12]
EIM_A24 [12]
LIB_L [15]
CSPI1_CLK [15]
CSPI1_MISO [15]
CSPI1_MOSI [15]
CSPI1_CS1 [15]
CSPI4_CS0 [14]
CSPI4_SCLK [14]
CSPI4_MISO [14]
UART3_CTS_L [15]
UART3_TX [15]
UART3_RX [15]
UART2_TX [15]
UART2_RX [15]
CSPI4_MOSI [14]
USB1_EN_OC_L [15]
UART3_RTS_L [15]
CSPI1_CS0 [12,15]
EIM_EB3 [12]
EIM_BCLK [15]
EIM_WAIT [12]
EIM_EB0 [12]
EIM_EB1 [12]
EIM_DA0 [12]
EIM_DA1 [12]
EIM_DA2 [12]
EIM_DA3 [12]
EIM_DA4 [12]
EIM_DA5 [12]
EIM_DA6 [12]
EIM_DA7 [12]
EIM_DA8 [12]
EIM_DA9 [12]
EIM_DA10 [12]
EIM_DA11 [12]
EIM_DA12 [12]
LCD_BACKLIGHT_EN [12,15]
EIM_DA14 [12]
EIM_DA15 [12]
U1D
i.MX6Q - DISP; CSI
NVCC_CSI
NVCC_LCD
NVCC_MIPI
CSI0_MCLK P4
CSI0_PIXCLK P1
CSI0_VSYNC N2
CSI0_DATA_EN P3
CSI0_DAT4 N1
CSI0_DAT5 P2
CSI0_DAT6 N4
CSI0_DAT7 N3
CSI0_DAT8 N6
CSI0_DAT9 N5
CSI0_DAT10 M1
CSI0_DAT11 M3
CSI0_DAT12 M2
CSI0_DAT13 L1
CSI0_DAT14 M4
CSI0_DAT15 M5
CSI0_DAT16 L4
CSI0_DAT17 L3
CSI0_DAT18 M6
CSI0_DAT19 L6
[15] PCAM_HSYNC
[15] PCAM_PXL_CK0
[15] PCAM_VSYNC
[15] PCAM_DE
[15] AUD3_TXC
[15] AUD3_TXD
[15] AUD3_TXFS
[15] AUD3_RXD
[15] I2C1_SDA
[15] I2C1_SCL
[15] PCAM_D0
[15] PCAM_D1
[15] PCAM_D2
[15] PCAM_D3
[15] PCAM_D4
[15] PCAM_D5
[15] PCAM_D6
[15] PCAM_D7
[15] PCAM_D8
[15] PCAM_D9
CSI_CLK0M F4
CSI_CLK0P F3
CSI_D0M E4
CSI_D0P E3
CSI_D1M D1
CSI_D1P D2
CSI_D2M E1
CSI_D2P E2
CSI_D3M F2
CSI_D3P F1
CSI_REXT D4
[15] CSI0_CK_N
[15] CSI0_CK_P
[15] CSI0_D0_N
[15] CSI0_D0_P
[15] CSI0_D1_N
[15] CSI0_D1_P
R515 6.04K
DI0_DISP_CLK N19
DI0_PIN2 N25
DI0_PIN3 N20
DI0_PIN4 P25
DI0_PIN15 N21
DISP0_DAT0 P24
DISP0_DAT1 P22
DISP0_DAT2 P23
DISP0_DAT3 P21
DISP0_DAT4 P20
DISP0_DAT5 R25
DISP0_DAT6 R23
DISP0_DAT7 R24
DISP0_DAT8 R22
DISP0_DAT9 T25
DISP0_DAT10 R21
DISP0_DAT11 T23
DISP0_DAT12 T24
DISP0_DAT13 R20
DISP0_DAT14 U25
DISP0_DAT15 T22
DISP0_DAT16 T21
DISP0_DAT17 U24
DISP0_DAT18 V25
DISP0_DAT19 U23
DISP0_DAT20 U22
DISP0_DAT21 T20
DISP0_DAT22 V24
DISP0_DAT23 W24
DSI_CLK0M H3
DSI_CLK0P H4
DSI_D0M G2
DSI_D0P G1
DSI_D1M H2
DSI_D1P H1
DSI_REXT G4
R393 22R
DISP0_CLK [15]
DISP0_HSYNC [15]
DISP0_VSYNC [15]
DISP0_CNTRST [15]
DISP0_DEN [15]
DISP0_DATA[0..23] [15]
R517 6.04K
MCIMX6Q7CVT08AC
VDD_RTC
R587 10K
RST_IN_M
POR_B [4,15]
SW2_3V3
C331 0.01uF
R651 NI
R652 0R
U41
SN74LVC1G07DCKR
RESET_IN_L [15]
RST_OUT_M
R411 10K
C326 0.1uF
R406 10K
POR_B_CPU
R410 1.5K
C114 1uF
U8
RESET* VDD
GND SENSE
MR* CT
TPS3808G33DBVT
C327 0.1uF
C330 0.01uF
VDDSOC_CAP
C108 4.7uF
C109 0.22uF
VDDHIGH_CAP
C110 47uF
C111 4.7uF
C112 0.22uF
U1F
i.MX6Q - SATA
SATA_VP G13
SATA_VPH G12
SATA_RXP B14
SATA_RXM A14
SATA_TXM B12
SATA_TXP A12
SATA_REXT C14
IMX_SATA_RXP C290 0.01uF
IMX_SATA_RXM C291 0.01uF
IMX_SATA_TXM C292 0.01uF
IMX_SATA_TXP C293 0.01uF
SATA_RXP [15]
SATA_RXN [15]
SATA_TXN [15]
SATA_TXP [15]
R521 191R
MCIMX6Q7CVT08AC
VDDSOC_CAP
C113 4.7uF
C115 0.22uF
C336 1000pF
C334 100pF
VDDHIGH_CAP
C117 4.7uF
C119 0.22uF
C337 1000pF
C335 100pF
U1I
i.MX6Q - HDMI
HDMI_VP L7
HDMI_VPH M7
HDMI_REF J1
HDMI_RESREF
R523 1.6K
HDMI_HPD K1
HDMI_DDCCEC K2
HDMI_CLKM J5
HDMI_CLKP J6
HDMI_D0M K5
HDMI_D0P K6
HDMI_D1M J3
HDMI_D1P J4
HDMI_D2M K3
HDMI_D2P K4
R522 0R
HDMI_HPD [15]
HDMI_CLKM [15]
HDMI_CLKP [15]
HDMI_D0M [15]
HDMI_D0P [15]
HDMI_D1M [15]
HDMI_D1P [15]
HDMI_D2M [15]
HDMI_D2P [15]
MCIMX6Q7CVT08AC
U1C
MCIMX6Q7CVT08AC
i.MX6Q - CONTROL
VDD_SNVS_IN
NVCC_JTAG
ONOFF D12
POR_B C11
BOOT_MODE0 C12
BOOT_MODE1 F12
TEST_MODE E12
TAMPER E11
PMIC_STBY_REQ F11
PMIC_ON_REQ D11
XTALI A7
XTALO B7
RTC_XTALI D9
RTC_XTALO C9
JTAG_TCK H5
JTAG_TMS C3
JTAG_TDI G5
JTAG_TDO G6
JTAG_TRSTB C2
JTAG_MOD H6
R524 1K
[15] POWER_BTN_L
[12] BOOT_MODE0
[12] BOOT_MODE1
[12] TEST_L
[4] PMIC_STBY_REQ
[4] PMIC_ON_REQ
R574 10K
R435 NI
R596 2.2M
put this resistor near by ball A7
CLK1_N C7
CLK1_P D7
CLK2_N C5
CLK2_P D5
R637 33R
R638 33R
R635 49.9R
R636 49.9R
R642 1K
R643 1K
PCIE1_REFCLK_DN [15]
PCIE1_REFCLK_DP [15]
CLK1/2 is mode match circuit:
LVDS: Install R637=22ohm, R635=49.9ohm, R642=NI
HCSL: Install R637=0.1uF, R635=56ohm, R642=470ohm.
XTALO
XTALI
R139 0R
R525 1M
24MHz
Y3
C302 24pF
C301 24pF
RTC_XTALI
RTC_XTALO
R526 5.1M
Y1
32.768KHz
C123 18pF
C124 18pF
SW2_3V3
R408 4.7K
R409 4.7K
I2C1_SDA
I2C1_SCL
Design <design>
Review <review>
Authorize <authorize>
Standardize <standardize>
Title 07 IMX6Q_SOC_A
Size A3
Doc Name ET-SOMIMX6
Ver. V0.0
Date Friday, March 08, 2019
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Layout: High speed data lines : 50 ohms
Put the 33ohm resistors in this page near imx6Q

U1B MCIMX6Q7CVT08AC — i.MX6Q

U1K — i.MX6Q - RGMII — MCIMX6Q7CVT08AC

U1G — i.MX6Q - USB — MCIMX6Q7CVT08AC

U1H — i.MX6Q - LVDS — MCIMX6Q7CVT08AC

U1L — i.MX6Q - PCIe — MCIMX6Q7CVT08AC

Design	<design>	Title 08 IMX6Q_SOC_B
Review	<review>	
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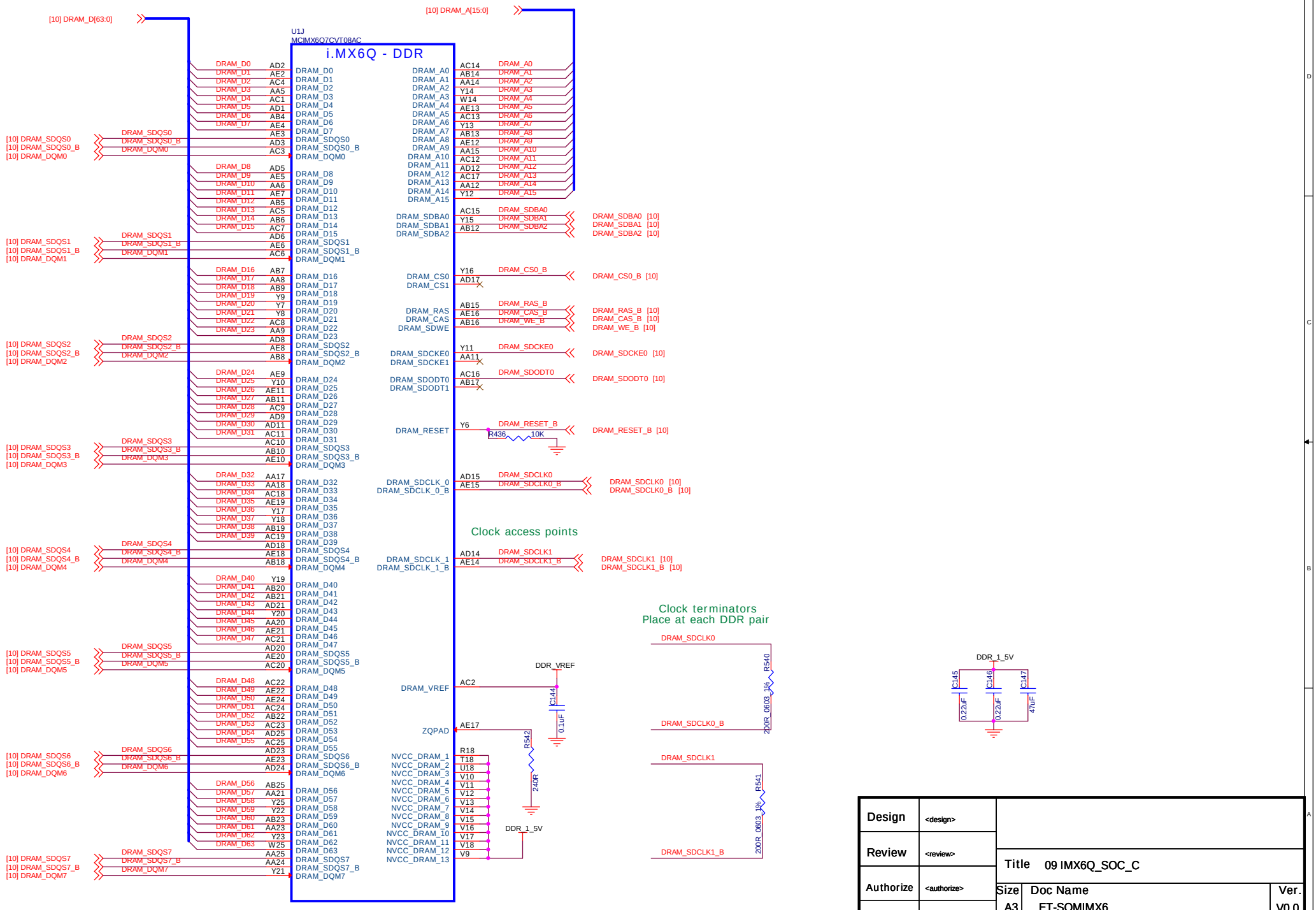
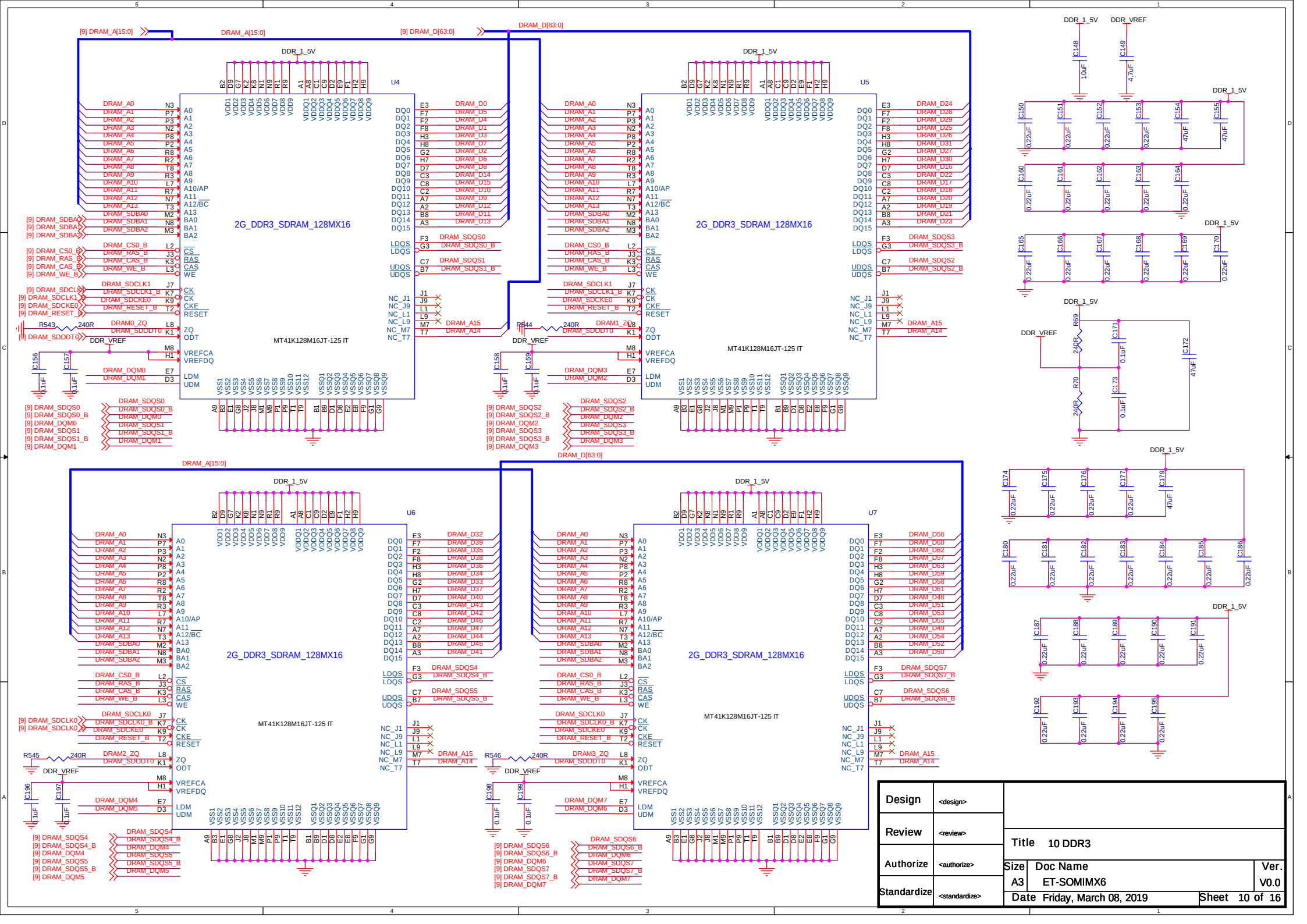
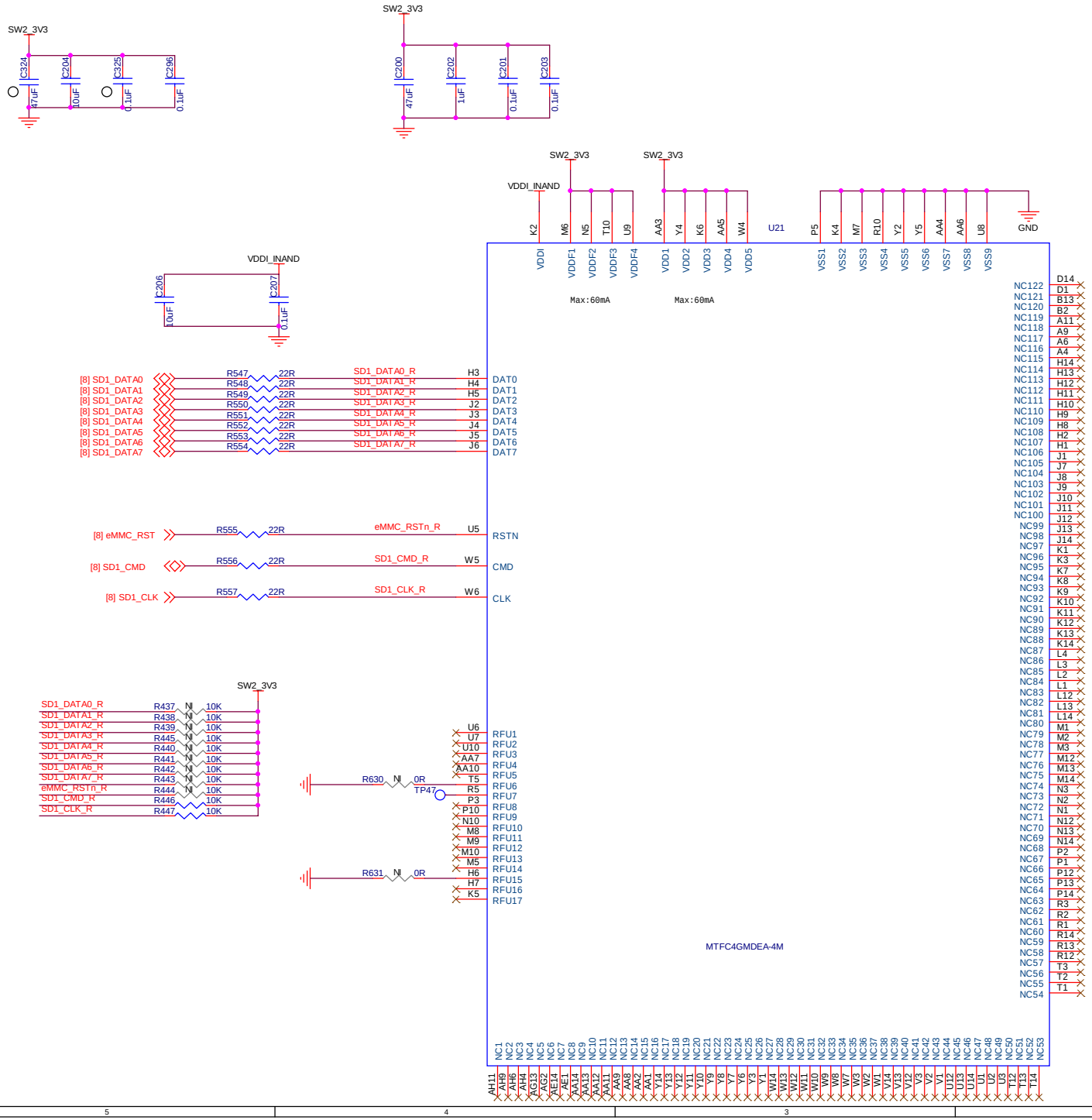
Standardize	<standardize>	Date Friday, March 08, 2019 Sheet 8 of 16



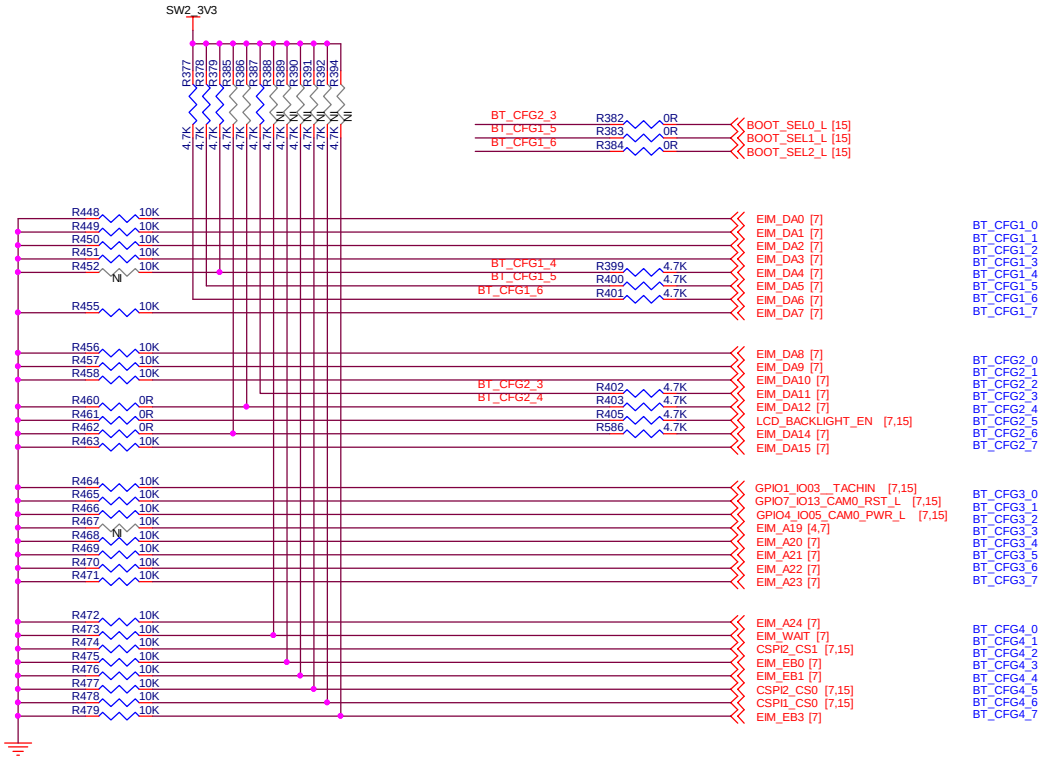
Design	<design>	Title	09 IMX6Q_SOC_C
Review	<review>		
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6 Ver. V0.0
Standardize	<standardize>	Date	Friday, March 08, 2019 Sheet 9 of 16



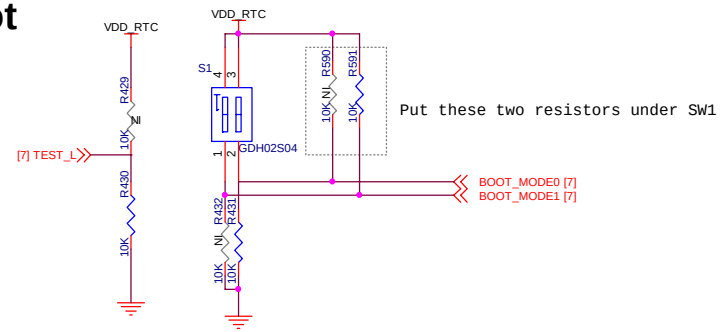
Design	<design>	Title	10 DDR3
Review	<review>	Size	A3
Authorize	<authorize>	Doc Name	ET-SOMIMX6
Standardize	<standardize>	Ver.	V0.0
		Date	Friday, March 08, 2019
		Sheet	10 of 16



Design	<design>	Title	11 eMMC
Review	<review>		
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6 Ver. V0.0
Standardize	<standardize>	Date	Friday, March 08, 2019 Sheet 11 of 16



Boot



CPU Boot Select Table

BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC / eMMC Boot				X0 = 1 - bit X1 = 4 - bit 10 = 8 - bit		00 = SD1 Boot 01 = SD2 Boot 11 = SD4 Boot	
010X = SD / eSD Boot				X0 = 1 - bit X1 = 4 - bit		00 = SD1 Boot 01 = SD2 Boot 11 = SD4 Boot	
0011 = SPI Boot				X	X	X	0

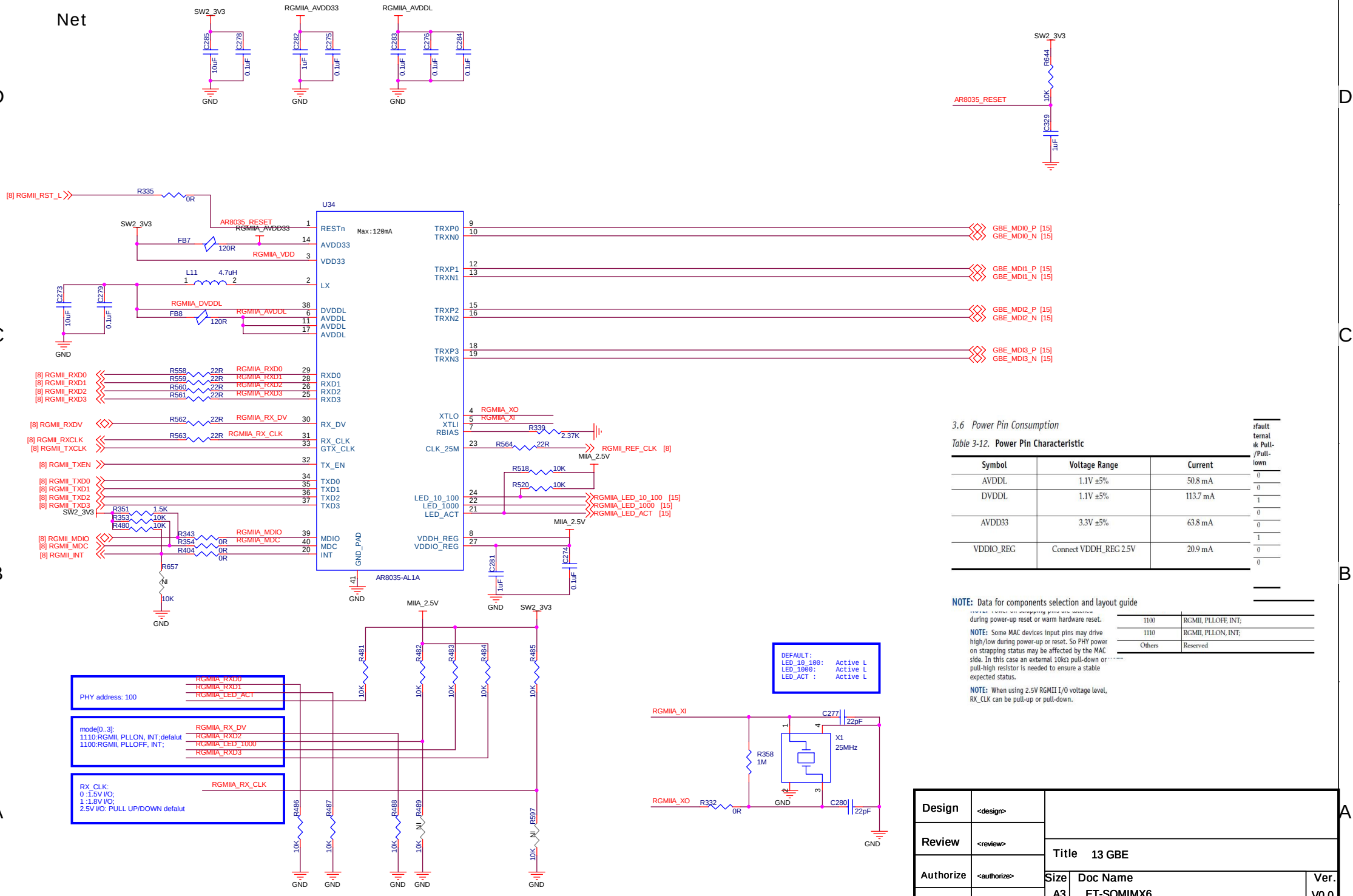
BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved

Carrier Boot Select:
011 Carrier SPI
101 Carrier SD
110 Module eMMC

1 means float on carrier

Design	<design>	Title	12 BOOT SELECT
Review	<review>		
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6 Ver. V0.0
Standardize	<standardize>	Date	Sunday, July 21, 2019 Sheet 12 of 16

Net



3.6 *Power Pin Consumption*

Table 3-12. **Power Pin Characteristic**

Symbol	Voltage Range	Current
AVDDL	1.1V ±5%	50.8 mA
DVDDL	1.1V ±5%	113.7 mA
AVDD33	3.3V ±5%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

NOTE: Data for components selection and layout guide

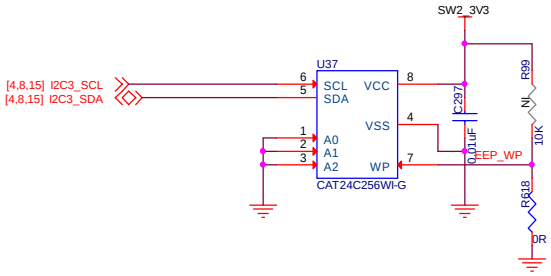
during power-up reset or warm hardware reset.

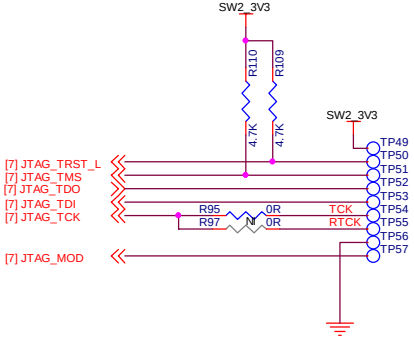
NOTE: Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10kΩ pull-down or pull-high resistor is needed to ensure a stable expected status.

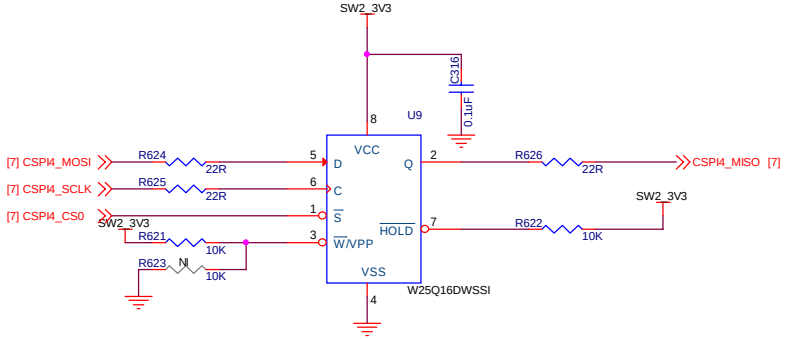
NOTE: When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

1100	RGMII, PLLOFF, INT;
1110	RGMII, PLLON, INT;
Others	Reserved

Design	<design>	Title	13 GBE
Review	<review>		
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6
Standardize	<standardize>	Date	Friday, March 08, 2019
			Ver. V0.0
		Sheet	13 of 16







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Review	<review>	Title 14 EEPROM & JTAG		
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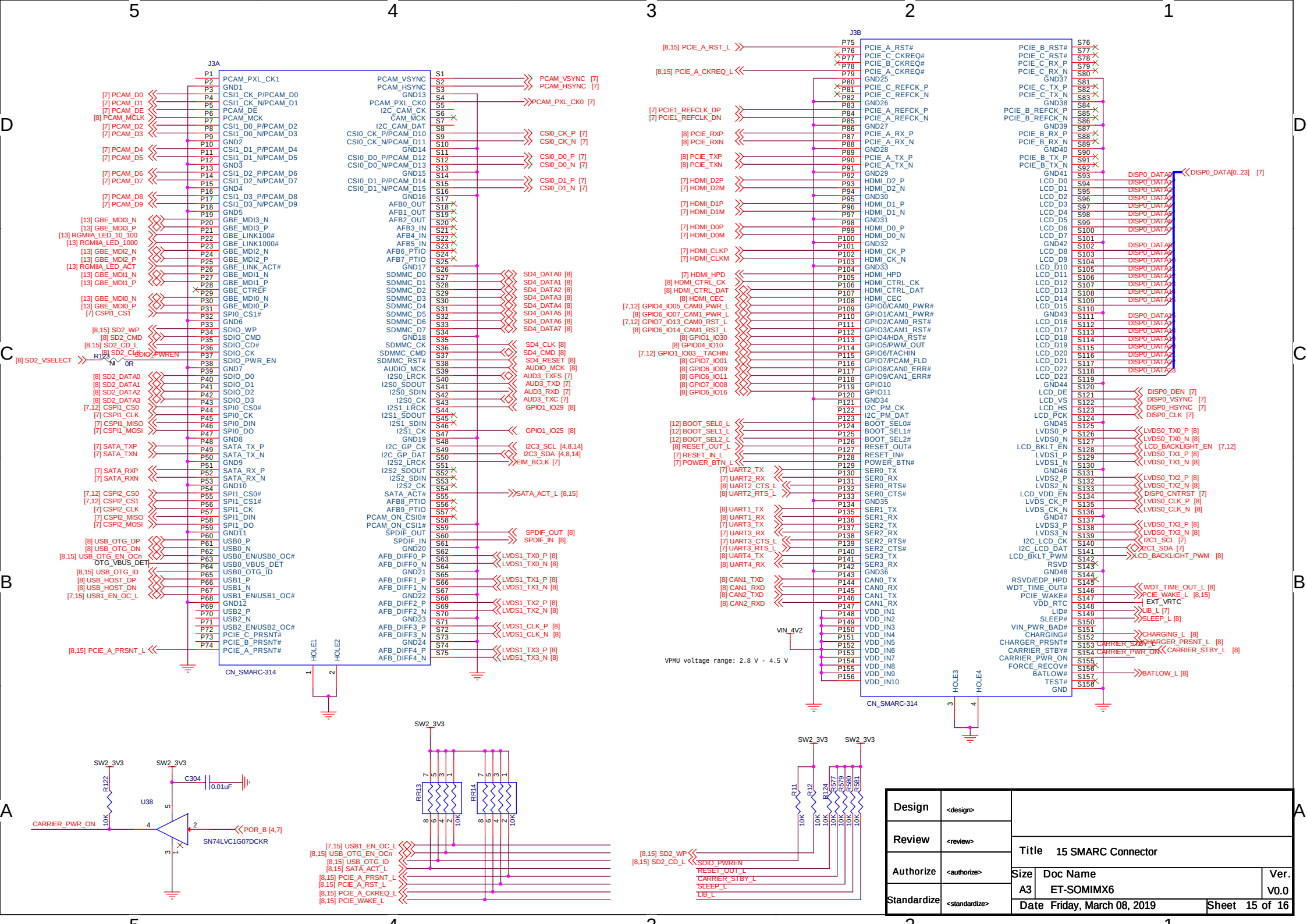
Standardize	<standardize>	Date Monday, March 11, 2019	Sheet 14 of 16	


J3A
CN_SMARC-314
J3B
CN_SMARC-314
SN74LVC1G07DCKR
VPMU voltage range: 2.8 V - 4.5 V
Design
Review
Authorize
Standardize
Title 15 SMARC Connector
Size A3
Doc Name ET-SOMIMX6
Ver. V0.0
Date Friday, March 08, 2019
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Schematic History

REV	Description	DATE	BY
V00	Initial production Release.		

Design	<design>		
Review	<review>	Title 16 Design History	
Authorize	<authorize>	Size A3	Doc Name ET-SOMIMX6 / Ver. V0.0
Standardize	<standardize>	Date Friday, March 08, 2019	Sheet 16 of 16