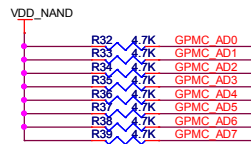
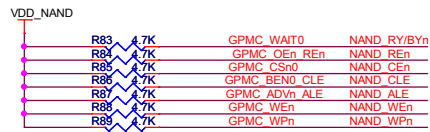
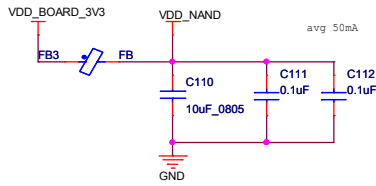


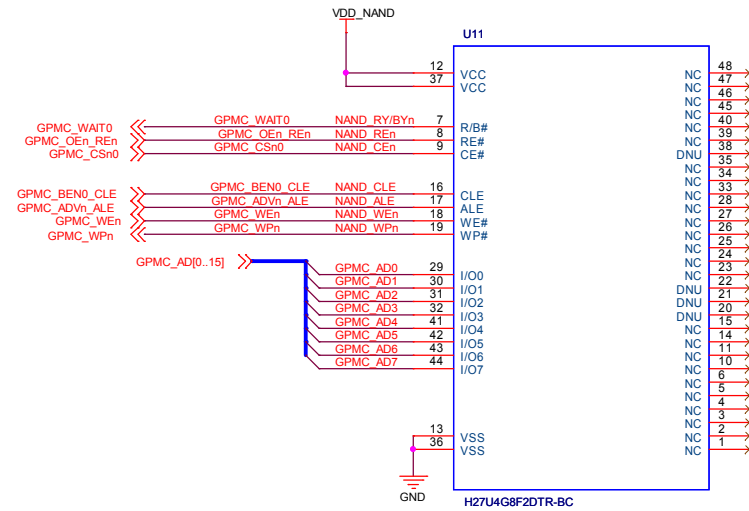
MINI8600B 120900

- 01 INDEX PAGE
- 02 BLOCK
- 03 INSTRUCTION
- 04 PWR
- 05 AM335XZCZ-DDR-NAND
- 06 AM335XZCZ-LCD-UART-I2C-MCASP
- 07 AM335XZCZ-PWR
- 08 DDR
- 09 MMC& EEROM
- 10 AM335XZCZ-CON
- 11 REVISION HISTORY

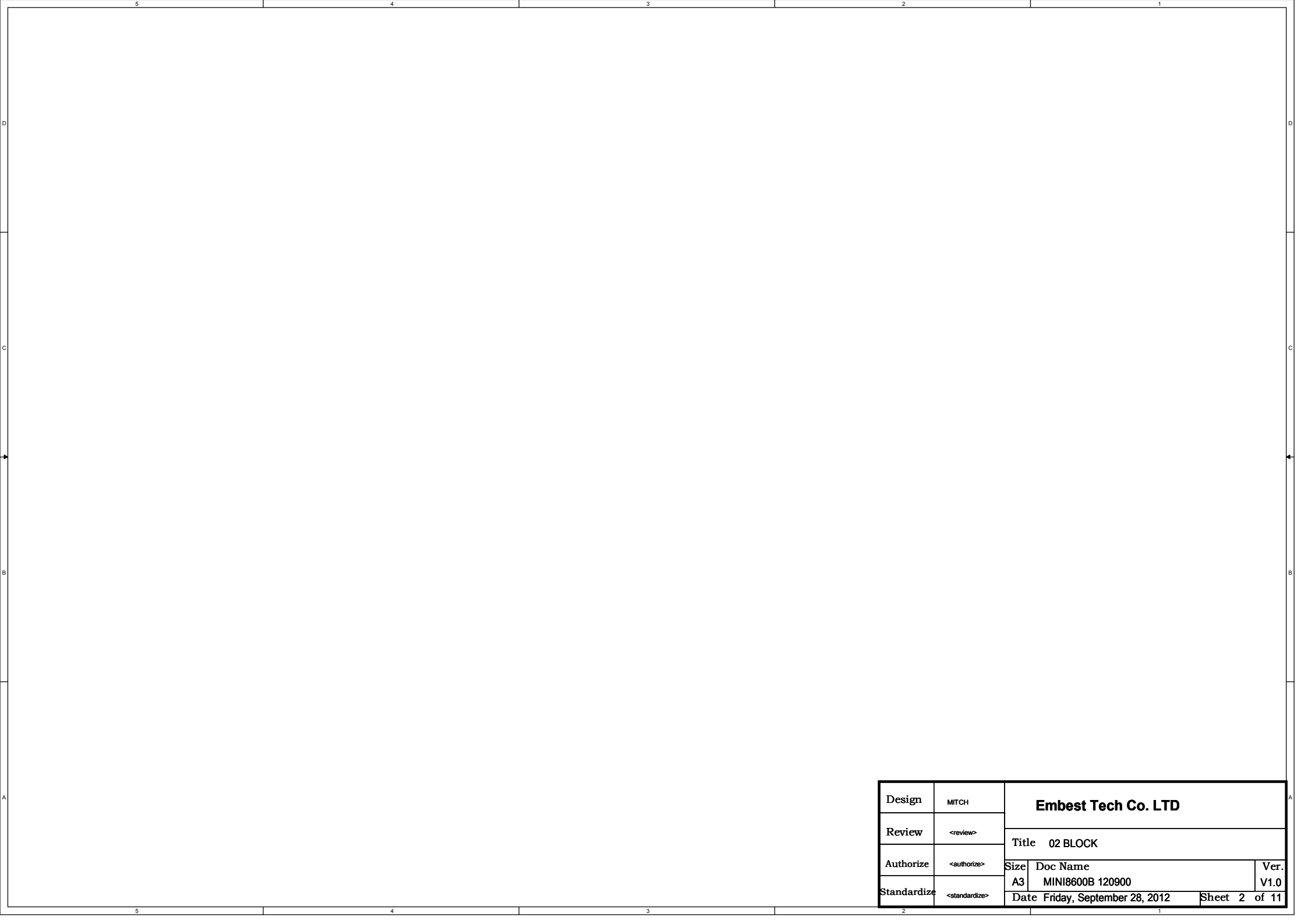
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Standardize	<standardize>	A3	MINI8600B 120900	V1.0
		Date	Friday, September 28, 2012	Sheet 1 of 11



if space careless, serial resistors recommended(22R) on data[0..7]



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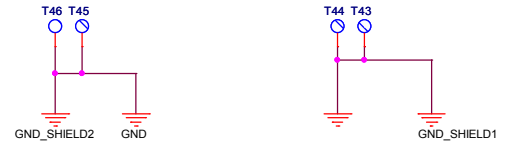
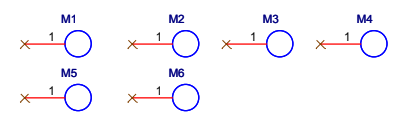
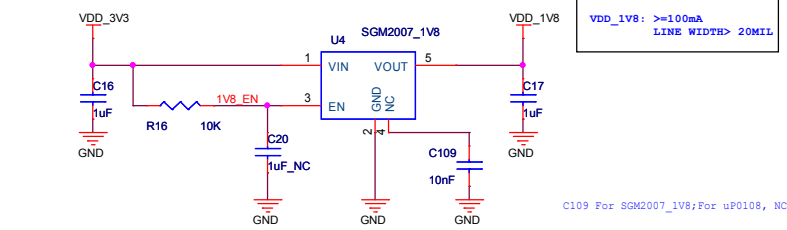
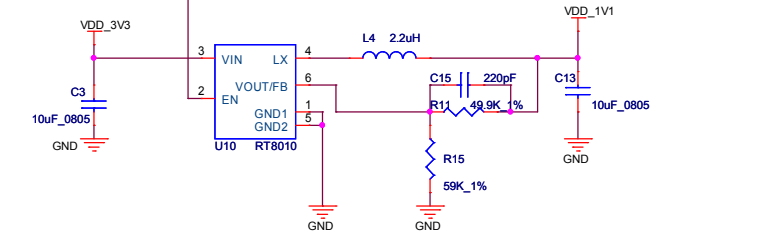
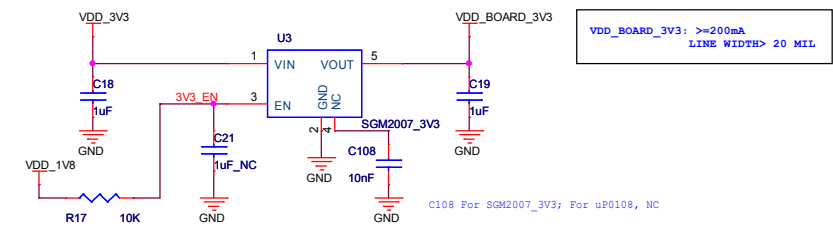
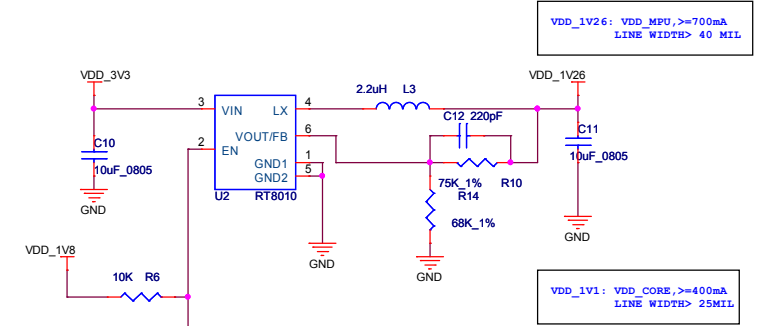
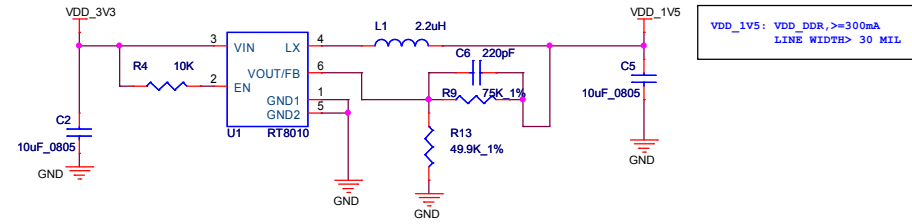
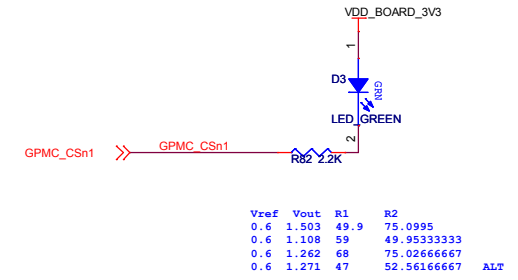
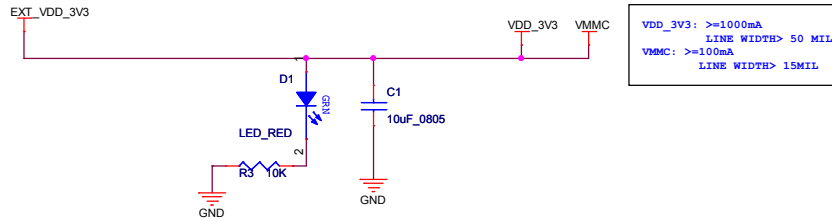
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HARDWARE INSTRUCTION

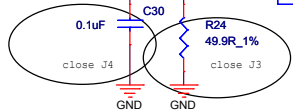
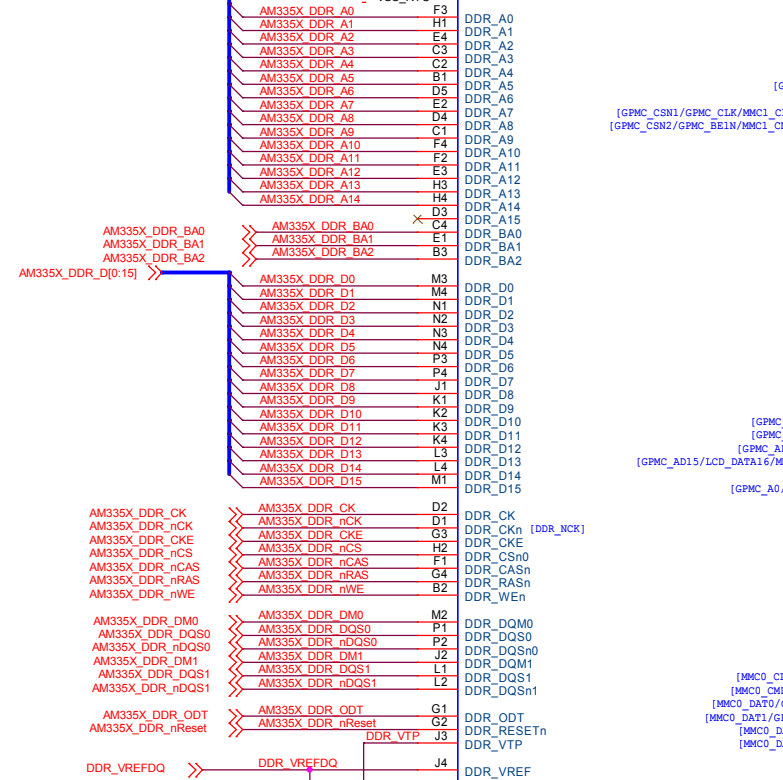
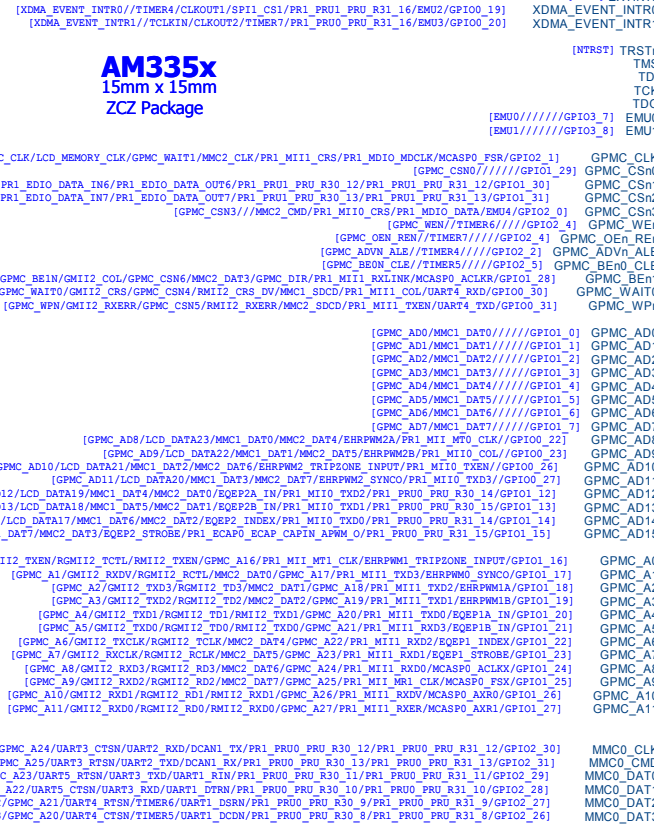
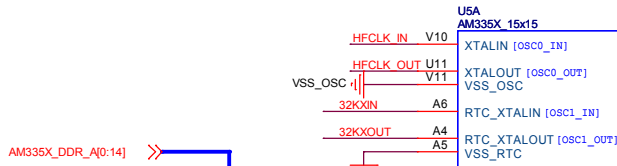
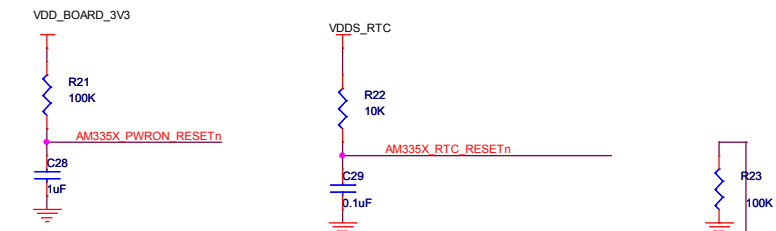
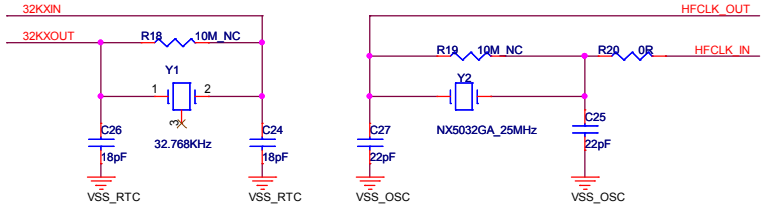
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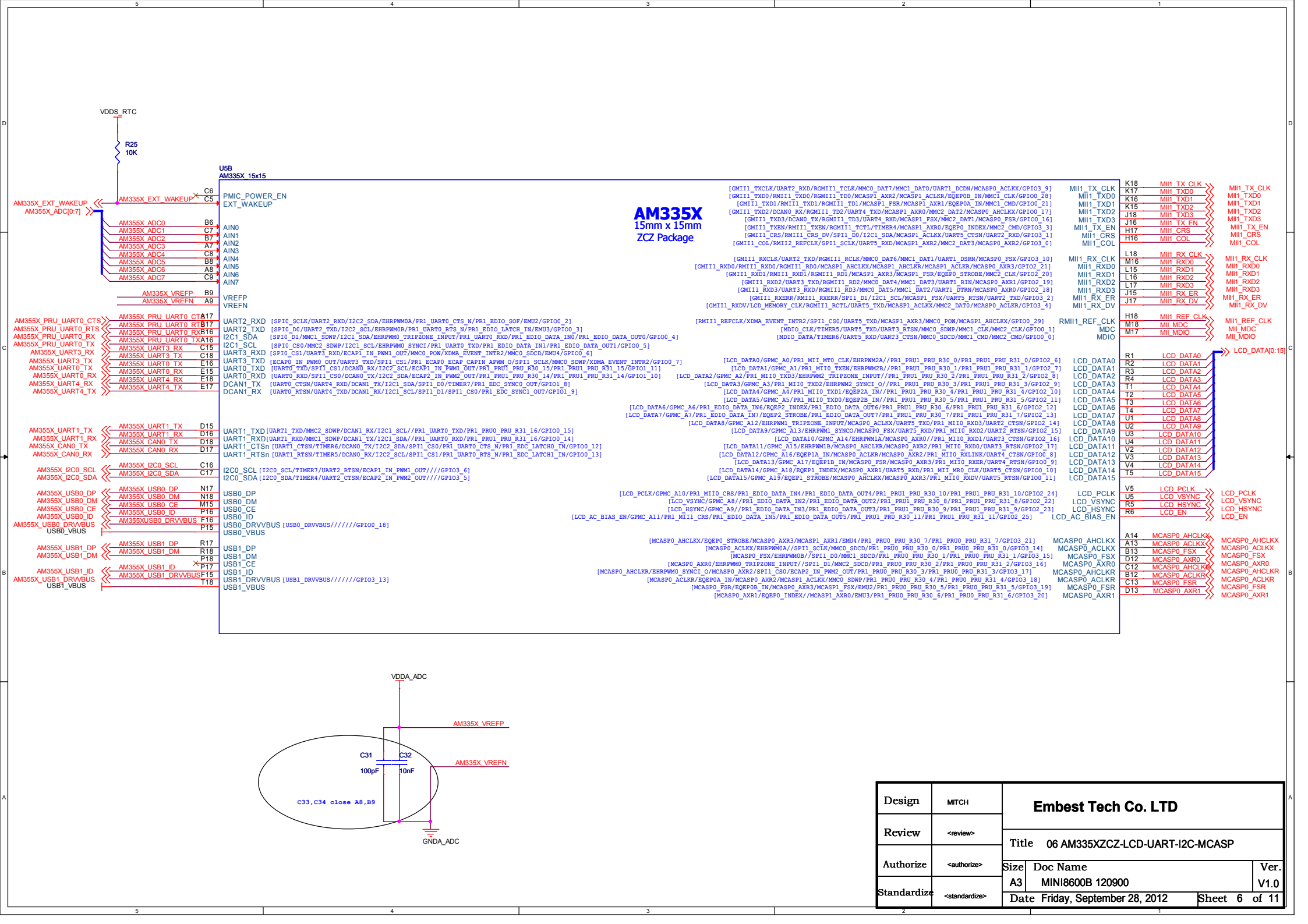
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		Date Friday, September 28, 2012		



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		Date	Friday, September 28, 2012	Sheet 5 of 11



**AM335X
15mm x 15mm
ZCZ Package**

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[GMII1_TXCLK/UART2_RXD/RGMII1_TCLK/MMC0_DAT7/MMC1_DAT0/UART1_DCDN/MCASPO_ACLKX/GPIO3_9] MIH1_TX_CLK
[GMII1_TXD0/RMII1_TXD0/RGMII1_TD0/MCASP1_AKR2/MCASP1_ACLKR/EQEP0B_IN/MMC1_CLK/GPIO0_28] MIH1_TXD0
[GMII1_TXD1/RMII1_TXD1/RGMII1_TD1/MCASP1_AKR1/EQEP0A_IN/MMC1_CMD/GPIO0_21] MIH1_TXD1
[GMII1_TXD2/DCANO_RX/RGMII1_TD2/UART4_TXD/MCASP1_AKR0/MC2_DAT2/MCASPO_AHCLKX/GPIO0_17] MIH1_TXD2
[GMII1_TXD3/DCANO_TX/RGMII1_TD3/UART4_RXD/MCASP1_FSR/MMC2_DAT1/MCASPO_FSR/GPIO0_16] MIH1_TXD3
[GMII1_TXEN/RMII1_TXEN/RGMII1_TCTL/TIMER4/MCASP1_AKR0/EQEP0_INDEX/MMC2_CMD/GPIO3_3] MIH1_TX_EN
[GMII1_CRS/RMII1_CRS_DV/SP11_D0/I2C1_SDA/MCASP1_ACLKX/UART5_CTSN/UART2_RXD/GPIO3_1] MIH1_CRS
[GMII1_COL/RMII2_REFCLK/SP11_SCLK/UART5_RXD/MCASP1_AKR2/MMC2_DAT3/MCASPO_AKR2/GPIO3_0] MIH1_COL

[GMII1_RXCLK/UART2_TXD/RGMII1_RCLK/MMC0_DAT5/MMC1_DAT1/UART1_DSN/MCASPO_FSR/GPIO3_10] MIH1_RX_CLK
[GMII1_RXD0/RMII1_RXD0/RGMII1_RD0/MCASP1_AHCLKX/MCASP1_AHCLKR/MCASP1_ACLKR/MCASPO_AKR3/GPIO2_21] MIH1_RXD0
[GMII1_RXD1/RMII1_RXD1/RGMII1_RD1/MCASP1_AKR3/MCASP1_FSR/EQEP0_STROBE/MMC2_CLK/GPIO2_20] MIH1_RXD1
[GMII1_RXD2/UART3_TXD/RGMII1_RD2/MMC0_DAT4/MMC1_DAT3/UART1_RIN/MCASPO_AKR1/GPIO2_19] MIH1_RXD2
[GMII1_RXD3/UART3_RXD/RGMII1_RD3/MMC0_DAT5/MMC1_DAT2/UART1_DTRN/MCASPO_AKR0/GPIO2_18] MIH1_RXD3
[GMII1_RXERR/RMII1_RXERR/SP11_DI/I2C1_SCL/MCASP1_FSR/UART5_RTSN/UART2_TXD/GPIO3_2] MIH1_RX_ER
[GMII1_RXD0/LCD_MEMORY_CLK/RGMII1_RCTL/UART5_TXD/MCASP1_ACLKX/MMC2_DAT0/MCASPO_ACLKR/GPIO3_4] MIH1_RX_DV

[RMII1_REFCLK/XDMA_EVENT_INTR2/SP11_CSO/UART5_TXD/MCASP1_AKR3/MMC0_POW/MCASP1_AHCLKX/GPIO0_29] RMII1_REF_CLK
[MDIO_DATA/TIMER6/UART5_RXD/UART3_CTSN/MMC0_SDCD/MMC1_CMD/MMC2_CMD/GPIO0_0] MDIO

[LCD_DATA0/GPMC_A0/PR1_MII_MIO_CLK/EHRPWM2A_/PR1_PRU1_PRU_R30_0/PR1_PRU1_PRU_R31_0/GPIO2_6] LCD_DATA0
[LCD_DATA1/GPMC_A1/PR1_MII0_TXEN/EHRPWM2B_/PR1_PRU1_PRU_R30_1/PR1_PRU1_PRU_R31_1/GPIO2_7] LCD_DATA1
[LCD_DATA2/GPMC_A2/PR1_MII0_TXD3/EHRPWM2_TRIPZONE_INPUT_/PR1_PRU1_PRU_R30_2/PR1_PRU1_PRU_R31_2/GPIO2_8] LCD_DATA2
[LCD_DATA3/GPMC_A3/PR1_MII0_TXD2/EHRPWM2_SYNCI_0_/PR1_PRU1_PRU_R30_3/PR1_PRU1_PRU_R31_3/GPIO2_9] LCD_DATA3
[LCD_DATA4/GPMC_A4/PR1_MII0_TXD1/EQEP2A_IN_/PR1_PRU1_PRU_R30_4/PR1_PRU1_PRU_R31_4/GPIO2_10] LCD_DATA4
[LCD_DATA5/GPMC_A5/PR1_MII0_TXD0/EQEP2B_IN_/PR1_PRU1_PRU_R30_5/PR1_PRU1_PRU_R31_5/GPIO2_11] LCD_DATA5
[LCD_DATA6/GPMC_A6/PR1_EDIO_DATA_IN6/EQEP2_INDEX/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_6/PR1_PRU1_PRU_R31_6/GPIO2_12] LCD_DATA6
[LCD_DATA7/GPMC_A7/PR1_EDIO_DATA_IN7/EQEP2_STROBE/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_7/PR1_PRU1_PRU_R31_7/GPIO2_13] LCD_DATA7
[LCD_DATA8/GPMC_A12/EHRPWM1_TRIPZONE_INPUT/MCASPO_ACLKX/UART5_TXD/PR1_MII0_RXD2/UART2_CTSN/GPIO2_14] LCD_DATA8
[LCD_DATA9/GPMC_A13/EHRPWM1_SYNCO/MCASPO_FSR/UART5_RXD/PR1_MII0_RXD2/UART2_RTSN/GPIO2_15] LCD_DATA9
[LCD_DATA10/GPMC_A14/EHRPWM1A/MCASPO_AXR0_/PR1_MII0_RXD1/UART3_CTSN/GPIO2_16] LCD_DATA10
[LCD_DATA11/GPMC_A15/EHRPWM1B/MCASPO_AHCLKR/MCASPO_AKR2/PR1_MII0_RXD0/UART3_RTSN/GPIO2_17] LCD_DATA11
[LCD_DATA12/GPMC_A16/EQEP1A_IN/MCASPO_ACLKR/MCASPO_AKR2/PR1_MII0_RXLINK/UART4_CTSN/GPIO0_8] LCD_DATA12
[LCD_DATA13/GPMC_A17/EQEP1B_IN/MCASPO_FSR/MCASPO_AKR3/PR1_MII0_RXERR/UART4_RTSN/GPIO0_9] LCD_DATA13
[LCD_DATA14/GPMC_A18/EQEP1_INDEX/MCASPO_AKR1/UART5_RXD/PR1_MII0_CLK/UART5_CTSN/GPIO0_10] LCD_DATA14
[LCD_DATA15/GPMC_A19/EQEP1_STROBE/MCASPO_AHCLKX/MCASPO_AKR3/PR1_MII0_RXD0/UART5_RTSN/GPIO0_11] LCD_DATA15

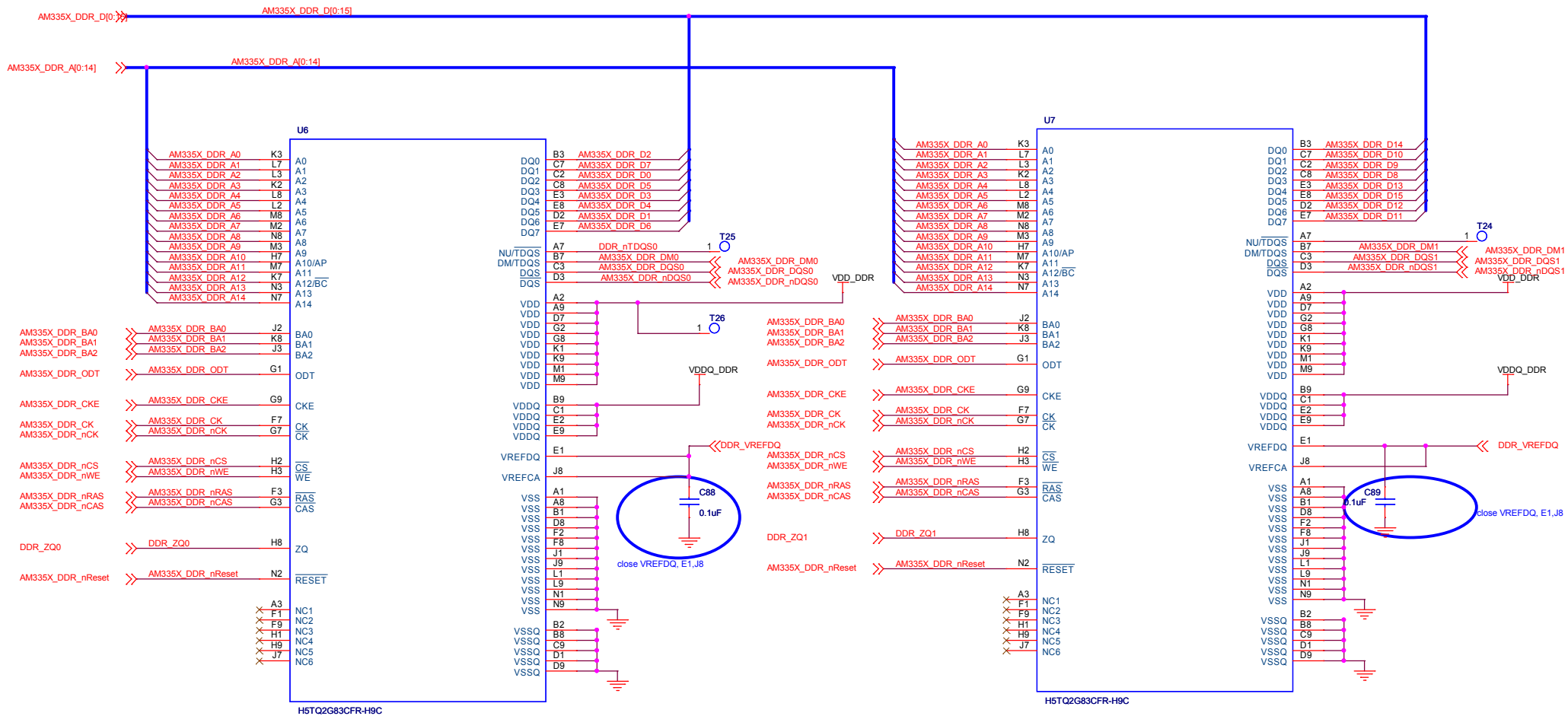
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[LCD_VSYNC/GPMC_A8_/PR1_EDIO_DATA_IN2/PR1_EDIO_DATA_OUT2/PR1_PRU1_PRU_R30_8/PR1_PRU1_PRU_R31_8/GPIO2_22] LCD_VSYNC
[LCD_HSINC/GPMC_A9_/PR1_EDIO_DATA_IN3/PR1_EDIO_DATA_OUT3/PR1_PRU1_PRU_R30_9/PR1_PRU1_PRU_R31_9/GPIO2_23] LCD_HSINC
[LCD_AC_BIAS_EN/GPMC_A11/PR1_MII1_CRS/PR1_EDIO_DATA_IN5/PR1_EDIO_DATA_OUT5/PR1_PRU1_PRU_R30_11/PR1_PRU1_PRU_R31_11/GPIO2_25] LCD_AC_BIAS_EN

[MCASPO_AHCLKX/EQEP0_STROBE/MCASPO_AKR3/MCASP1_AKR1/EMU4/PR1_PRU0_PRU_R30_7/PR1_PRU0_PRU_R31_7/GPIO3_21] MCASPO_AHCLKX
[MCASPO_ACLKX/EHRPWM0A_/SP11_SCLK/MMC0_SDCD/PR1_PRU0_PRU_R30_0/PR1_PRU0_PRU_R31_0/GPIO3_14] MCASPO_ACLKX
[MCASPO_FSR/EHRPWM0B_/SP11_D0/MMC1_SDCD/PR1_PRU0_PRU_R30_1/PR1_PRU0_PRU_R31_1/GPIO3_15] MCASPO_FSR
[MCASPO_AXR0/EHRPWM0_TRIPZONE_INPUT_/SP11_DI/MMC2_SDCD/PR1_PRU0_PRU_R30_2/PR1_PRU0_PRU_R31_2/GPIO3_16] MCASPO_AXR0
[MCASPO_AHCLKR/EHRPWM1_SYNCI_0_/MCASPO_AXR2/SP11_CSO/EQEP2_IN_PWM2_OUT/PR1_PRU0_PRU_R30_3/PR1_PRU0_PRU_R31_3/GPIO3_17] MCASPO_AHCLKR
[MCASPO_AHCLKR/EHRPWM1_SYNCO/MCASPO_AKR2/MCASP1_ACLKR/MMC0_SDCD/PR1_PRU0_PRU_R30_4/PR1_PRU0_PRU_R31_4/GPIO3_18] MCASPO_AHCLKR
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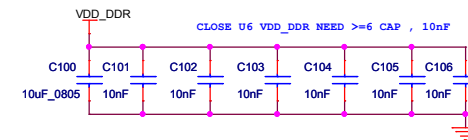
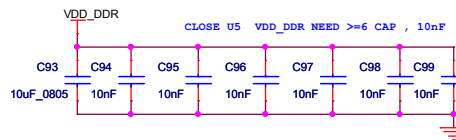
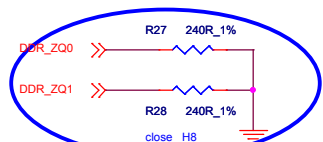
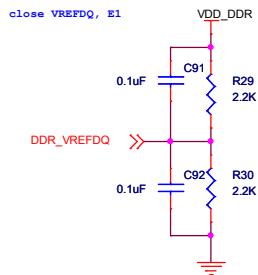
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 K17 MIH1_TXD0
 K16 MIH1_TXD1
 K15 MIH1_TXD2
 J18 MIH1_TXD3
 MIH1_TX_EN
 H17 MIH1_CRS
 H16 MIH1_COL
 L18 MIH1_RX_CLK
 M16 MIH1_RXD0
 L15 MIH1_RXD1
 L16 MIH1_RXD2
 L17 MIH1_RXD3
 J15 MIH1_RX_ER
 J17 MIH1_RX_DV
 H18 MIH1_REF_CLK
 M18 MIH1_MDC
 M17 MIH1_MDIO
 R1 LCD_DATA0
 R2 LCD_DATA1
 R3 LCD_DATA2
 R4 LCD_DATA3
 R11 LCD_DATA4
 T2 LCD_DATA5
 T3 LCD_DATA6
 T4 LCD_DATA7
 U1 LCD_DATA8
 U2 LCD_DATA9
 U3 LCD_DATA10
 U4 LCD_DATA11
 V2 LCD_DATA12
 V3 LCD_DATA13
 V4 LCD_DATA14
 T5 LCD_DATA15
 U5 LCD_PCLK
 U6 LCD_VSYNC
 R5 LCD_HSINC
 R6 LCD_EN
 A14 MCASPO_AHCLKX
 A13 MCASPO_ACLKX
 B13 MCASPO_FSR
 D12 MCASPO_AXR0
 C12 MCASPO_AHCLKR
 B12 MCASPO_ACLKR
 C13 MCASPO_FSR
 D13 MCASPO_AKR1
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 MIH1_TXD0
 MIH1_TXD1
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 MIH1_TXD3
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 MIH1_CRS
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Ver.					V1.0

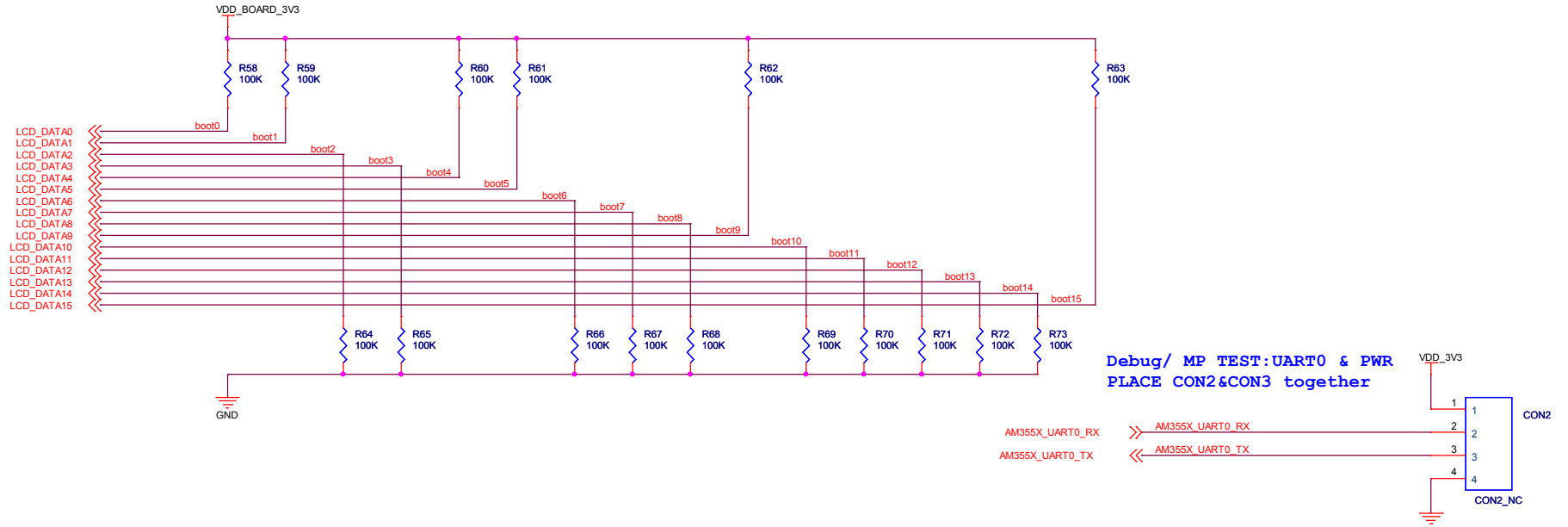


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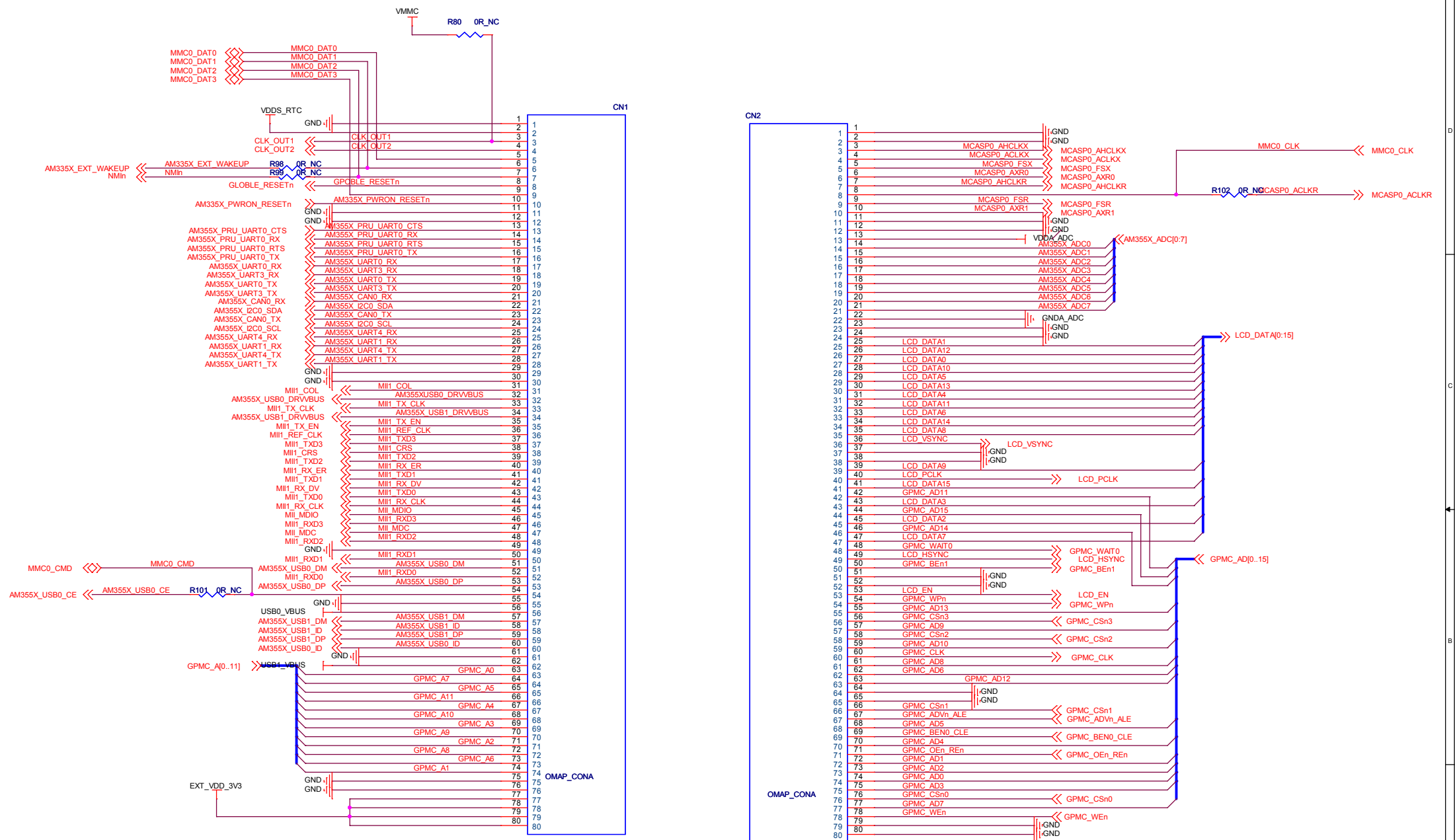


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		Date	Friday, September 28, 2012	Sheet 8 of 11

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 BOOT[4...0]: 10011 NAND-NANDI2C-MMC0-UART0 || 10111 MMC0->SPI0->UART0->USB0
 BOOT[5]: 1b CLKOUT1=enable
 BOOT[7,6]:00b MII
 BOOT[8]: 0b 8BIT NAND
 BOOT[9]: 1b ECC by NAND
 BOOT[11,10]:00b for NAND
 BOOT[13,12]: 00b by default
 BOOT[15,14]: 10b 25MHz



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MINI8600B Revision History

MINI8600B 110900

1 Modify From MINI8600 0601, Add Nand;RM TF card .

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